Study on Structural, Optical and Electrical Properties of Single Junction Mono-crystalline Silicon Solar Cells

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Nahid Akter

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Under the supervision of

Professor Dr. Zahid Hasan Mahmood

Electrical and Electronic Engineering
University of Dhaka, Dhaka-1000, Bangladesh

Professor Dr. Nowshad Amin

Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia (UKM)
Bangi, Selangor 43600, Malaysia

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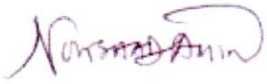
Originality Statement

I hereby declare that this submission is the own work of Ms. Nahid Akter and to the best of my knowledge it contains no materials previously published or written by another person, or substantial proportions of material which have been accepted for the award of any other degree or diploma at the University of Dhaka or any educational institution, except where due acknowledgement is made in the thesis. Any contribution made to the research by others, with whom Ms. Nahid Akter has worked at University of Dhaka or elsewhere, is explicitly acknowledged in the thesis. I also declare that intellectual content of this thesis is the product of Ms. Nahid Akter's research work, except to the extent that assistance from others is acknowledged.

Supervisor

Professor Dr. Zahid Hasan Mahmood
Dept. of Electrical and Electronic Engineering
University of Dhaka, Dhaka-1000, Bangladesh

Co-supervisor



Professor Dr. Nowshad Amin
Dept. of Electrical, Electronic and Systems Engineering
Faculty of Engineering and Built Environment
Universiti Kebangsaan Malaysia (UKM)
Bangi, Selangor 43600, Malaysia

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Abstract

The gap between laboratory scale and commercial silicon solar cells is wider as many standard processes are not being practiced in transforming to commercialization. The main objective of this work is to investigate the standard as well as simplified fabrication process applicability to commercially available low-cost silicon wafers. Therefore, it is urgently needed to put an intermediate step in between lab-scale fabrication and fully automated commercial facilities or processes. Eventually, smaller fabrication facilities may be benefitted from these comparative studies and get involved in more human resource extensive with commercially available low-cost silicon wafer. Efficiency was achieved to be 5.96% which proves viability of the approach. This study mainly focused on the investigation of effects of standard fabrication processes to commercially available low-cost silicon wafers therefore conversion efficiency was just regarded as the benchmark. However, a series of other characterization found some correlation between processing steps and quality of layers/devices, which can be considered as the contribution of the study. The relatively lower efficiency was probably caused by the complete procedure in a non-cleanroom environment with in-housebuilt low cost instruments, where thorough optimization of the process is needed. Therefore, it is believed that the efficiency can be improved by the use of standard clean room, alternate procedure of edge isolation, improvement of rapid thermal annealing procedure etc. This work thus showed the bridging gap between small scale laboratory solar cells (crystalline silicon based) with the commercial prototypes produced from extensive knowledge in each processing steps.

Contents

Cover

Originality statement i

Acknowledgements ii

Abstract iv

Content vi

List of Figures xi

List of Tables xv

Nomenclature xvii

1 Introduction 1-22

1.1 Introduction 1

1.1 Energy resources and consumption 1

1.1.1 Fossil fuel 2

1.1.2 Nuclear fuel 3

1.1.3 Renewable energy 4

1.2 Photovoltaic (PV) technology: Past and present 6

1.3 Problem Statement 7

1.4 Research Objectives 8

1.5 Materials for Photovoltaics 8

1.6 Mono-crystalline silicon technology 10

1.7 Principle of solar cell operation 11

1.8 Efficiency of silicon solar cell 12

1.9 Review of Literature 13

1.10 Organization of thesis 16

1.11 References 18

2 Characterization techniques 23-36

2.1 Introduction 23

2.2 Measurement of thickness 23

	2.3	Optical reflectance	24
		2.3.1 Spectroscopic Reflectometer	24
		2.3.2 Spectral reflectance measurement (SRM)	26
	2.4	Surface Morphology	26
		2.4.1 Scanning Electron Microscopy (SEM)	24
		2.4.2 2D optical microscopy	27
	2.5	Surface roughness measurement by Stylus surface Profiler	28
	2.6	Compositional analysis by energy dispersive x-ray (EDX) spectroscopy	29
	2.7	Optical properties: Surface Photo Voltage Spectroscopy	29
	2.8	Electrical properties measurement by four point probe	31
	2.9	Light-current-voltage (LIV) tester for IV curve	32
	2.10	Summary	34
	2.11	References	35
3	**Characterization of wafer**		**37-53**
	3.1	Introduction	37
	3.2	Mono-crystalline silicon substrate	37
	3.3	Hot-point probe theory	39
	3.4	Setup for measurement with hot probe	40
	3.5	Material type measurement by hot probe	41
	3.6	Wafer thickness measurement by dial indicator	42
	3.7	Electrical properties measurement by four point probe	42
	3.8	Hot probe characteristic curve analysis	44
	3.9	Thermal effect on carrier concentration	45
		3.9.1 Equation for thermally excited charge carrier concentration and impurity concentration	45
		3.9.2 Results	46
		3.9.3 Thermally excited charge carrier concentration by using Poisson's equation	47
		3.9.4 Experimental Results	49
	3.10	Summary	51
	3.11	References	52

4 Properties of chemically etched silicon wafers 54-68

4.1 Introduction 54

4.2 Necessity for isotropic and anisotropic etching 54

4.3 RCA cleaning and texturing process 56

4.4 Thickness of textured silicon sample 58

4.4.1 Results 58

4.5 Structural characterization 58

4.5.1 2D optical imaging 59

4.5.2 Scanning electron microscope imaging 59

4.5.3 Pyramid height measurement by stylus surface Profilometer 61

4.5.3.1 Results 62

4.6 Optical Characterization 63

4.6.1 Light reflectivity measurement by Spectroscopic Reflectometer 63

4.6.1.1 Results 63

4.6.2 Light reflectivity measurement by Spectral Reflectance Measurement 65

4.6.2.1 Results 66

4.7 Summary 67

4.8 References 68

5 Fabrication and characterization of emitter layer in Silicon wafer 69-96

5.1 Introduction 69

5.2 Thermal diffusion process 70

5.2.1 Precautions before handling $POCl_3$ 72

5.2.2 Condition for $POCl_3$ diffusion 72

5.2.3 Temperature dependent sheet resistivity 75

5.2.4 Operation and process time 75

5.2.5 Single step for doping and surface passivation and ARC 77

5.2.6 Contamination control 77

5.2.7 Challenges for Cl_2 gas removal 78

5.3 Spin-on process 78

5.3.1 Precautions before handling P5O9 80

5.3.2 Operation and process time 80
5.3.2.1 Film grown by spin coater 80
5.3.2.2 Baking 81
5.3.2.3 Diffusion by RTP furnace 81
5.4 Dip coating by P5O9 83
5.5 Edge Isolation 85
5.6 List of samples for diffusion process 84
5.7 Properties of emitter layer in silicon wafer 85
5.7.1 Polarity measurement by hot probe 85
5.7.2 Measurement of doping uniformity with hot probe 86
5.7.3 Surface topography by scanning electron microscope 87
5.7.4 Energy dispersive x-ray spectroscopy (EDS) analysis 88
5.7.5 Optical Reflectance 90
5.7.6 Resistivity by four point probe measurement 91
5.7.7 Measurement of thickness 92
5.8 Summary 93
5.9 References 95

6 Measurement for carrier lifetime and conversion efficiency 97-115
6.1 Introduction 97
6.2 Metallization and co-firing 97
6.3 Minority carrier diffusion length 98
6.4 Measurement of minority carrier diffusion length through SPV 99
6.5 Carrier generation and recombination 99
6.6 Quantitative derivation of carrier generation and recombination 101
6.7 Experimental details 102
6.7.1 Minority carrier diffusion length 102
6.7.2 Minority carrier lifetime 105
6.7.3 Carrier generation and recombination 105

	6.8	Equivalent circuit for solar cell	109
	6.9	LIV setup for measurement	111
	6.10	Measurement of Conversion efficiency	111
	6.11	Summary	113
	6.12	References	114
7	**Conclusion**		**116**
	7.1	Summary	116
	7.2	Future Prospects	119

List of Figures

Chapter I

Figure 1.1 Global energy consumption at year 2013 1
Figure 1.2 Fossil fuel energy consumption on 1971 (% of total) 2
Figure 1.3 Fossil fuel energy consumption on 2013 (% of total) 3
Figure 1.4 Alternative and nuclear energy (% of total energy use) 4
Figure 1.5 Renewable energy potential in 2009 5
Figure 1.6 Price history of silicon PV cells in $ per watt 7
Figure 1.7 Bandgap and efficiencies for photovoltaic materials 9
Figure 1.8 Working principle of solar cell 12
Figure 1.9 Telstar communication satellite 14

Chapter II

Figure 2.1 Front view of dial indicator 24
Figure 2.2 Front view of spectroscopic reflectometer 25
Figure 2.3 Front view of surface reflectance measurement 26
Figure 2.4 Front view of Scanning electron microscope 27
Figure 2.5 (a) Front view of dektak stylus surface profiler (b)) Close view of stylus tip 28
Figure 2.6 (a) Front view of SPV spectroscopy (b)) Front view of stanford researc h 510 lock-in amplifier 30
Figure 2.7 (a) Four point probe (b)) Close view of four point probe 31
Figure 2.8 Front view of LIV efficiency measurement instrument 33

Chapter III

Figure 3.1 Two alternate block diagram of hot-point probe measurement system 39
Figure 3.2 A low cost, in house made hot probe setup 41
Figure 3.3 Hot probe characteristic curves for (a) sample-1 and (b) sample-2 44
Figure 3.4 Carrier mobility versus temperature for silicon 47

Chapter IV

Figure 4.1 Dissolved NaOH in water, release heat 56

Figure 4.2 RCA cleaning for silicon sample preparation 57

Figure 4.3 Texturing procedures for silicon sample 58

Figure 4.4 2D optical images with magnification 10x for sample-1 (a) SiCr Referenc e sample for calibration (b) raw silicon wafer (c) cleaned silicon wafer (d) textured silicon wafer 60

Figure 4.5 SEM images of silicon sample-1 (a) Raw wafer (b) Saw damage removed wafer (c) textured silicon wafer (d) textured wafer of silicon sample-2 61

Figure 4.6 Sample 1 (a) and (b) Surface roughness profile 62

Figure 4.7 Block diagram of spectroscopic reflectometer 63

Figure 4.8 (a) Reflectivity graph of SiCr reference sample for calibration. %Reflectivity Vs wavelength graph for silicon sample-1(650-800 nm) (b) %Reflectivity for raw silicon wafer is about 2.4% (c) %Reflectivity for cleaned silicon wafer is about 24% (d) %Reflectivity for textured silicon wafer is about 1% that is reduced by multiple reflection from the pyramid growth (e) Comparison of %reflectivity for raw, cleaned and textured silicon wafer. 65

Figure 4.9 %Reflectivity versus wavelength graph for silicon sample-1 (650-800nm) (a) %Reflectivity for raw silicon wafer is about 13% (b) %Reflectivity for cleaned silicon wafer is about 21% (c) %Reflectivity for textured silicon wafer is about 8% that was reduced by multiple reflection from the pyramid growth (d) Comparison of %reflectivity for raw, cleaned and textured silicon wafer. 67

Chapter V

Figure 5.1 Illustration of thermal diffusion (a) pre-deposition (b) drive-in 70

Figure 5.2 Wafer loading in the horizontal thermal diffusion system 71

Figure 5.3 Bubbler system 72

Figure 5.4 Graph for Bubbler temperature versus POCl3 vapor pressure 74

Figure 5.5 Graph for carrier gas flow versus pickup rate at three different bubbler temperatures 74

Figure 5.6 Temperature profile for growth of emitter layer by $POCl_3$ thermal diffusion 76

Figure 5.7 Image of in house doped mono-silicon wafers 77

Figure 5.8 Cl_2 gas exhaust system 78

Figure 5.9 Spin on doping system 79

Figure 5.10 Two step program on SPS Spin 150 spin coater 81
Figure 5.11 rpm versus time profile 81
Figure 5.12 Time versus annealing temperature profile 82
Figure 5.13 Diffusion Process inside the annealing furnace 83
Figure 5.14 Edge isolation mask screen 83
Figure 5.15 Wafer mapping for sample-1 (a) front surface (b) rear surface 87
Figure 5.16 Comparison between (a) textured and (b) phosphorus doped sample-1 88
Figure 5.17 EDS spectrum of doped sample-1 89
Figure 5.18 %Reflectivity versus Wavelength graph for sample-1 (a) Textured silicon sample (b) doped silicon sample 91

Chapter VI

Figure 6.1 (a) Screen printed rear surface by Al paste (b) Screen printed front surface by Ag paste (c) Co-firing process by belt furnace (d) Fabricated mono-silicon solar cell 98
Figure 6.2 V_{SPV} versus wavelength (λ) graph: an output from the SPV measurement 103
Figure 6.3 $(\frac{1}{V_{SPV}})$ versus $(\frac{1}{\alpha})$ graph 103
Figure 6.4 The straight line cut at -110 µm that gives the value of diffusion length 105
Figure 6.5 Carrier generation for sample-1 106
Figure 6.6 Carrier recombination for sample-1 107
Figure 6.7 Remaining carrier for sample-1 108
Figure 6.8 Total carrier generation and reconmbination rate for the entire thickness of sample-1 solar cell (left) and rest of the cell ignoring the surface (right) 108
Figure 6.9 A diode circuit model describing a PV cell connected to a source meter for IV testing 109
Figure 6.10 IV curve for a silicon PV cell 110
Figure 6.11 (a) Custom designed probes (b) Programmable current-voltage measurement power supply with LAB VIEW based interface 111
Figure 6.12 (a) I-V curve (b) P versus V curve for mono-silicon solar cell (125×125 mm^2) 112

Appendix I

Figure App 1: Front side view of De-ionized water plant 122
Figure App 2: (a) Front side view of laser cutter (b) Silicon wafer under the laser cutter 123
Figure App 3: (a) Front side view of fume hood (b) Basic parts of fume hood 124
Figure App 4: Front side view of sample cleaning bath 124
Figure App 5: Front side view of hot plate 125
Figure App 6: (a) Front side view of diffusion furnace (b) Motorized roller carry the wafer inside the horizontal diffusion furnace 126
Figure App 7: Front side view of spin coater 127
Figure App 8: Front side view of annealing furnace 128
Figure App 9: Screen printer 129
Figure App 10: Front side view of RTA belt furnace 130

List of Tables

Chapter I

Table 1.1 Properties of silicon 11

Table 1.2 Highest confirmed terrestrial solar cell efficiency measured under AM1.5 spectrum 13

Table 1.3 Major process steps, parameters and the monitoring techniques used in solar cell fabrication 16

Chapter III

Table 3.1 Sample name, Thicknesses and the supplier name 38

Table 3.2 Measurement of wafer type using indigenously made hot probe system 42

Table 3.3 Measurement of wafer thickness using dial indicator 42

Table 3.4 Resistivity measurement using four probe techniques 43

Table 3.5 Thermo-power measurement using hot probe characteristic curve 45

Table 3.6 Acceptor concentration at room temperature with respect to physical resistivity 47

Table 3.7 Temperature dependent hole mobility (μ_p), impurity concentration (N_A), function of heating temperature ® and thermally excited charge carrier density (Δp) 48

Table 3.8 Temperature dependent steady state voltage, hole diffusion coefficient (D_p) and thermally excited charge carrier (Q) 50

Table 3.9 Comparison between theoretical and experimental values of thermally excited charge carrier concentration 50

Chapter IV

Table 4.1: Thickness comparison table for raw and textured mono silicon sample 59

Table 4.2: Measurement of pyramid height using stylus surface profilometer 62

Chapter V

Table 5.1 Various gas flow rate for APCVD thermal diffusion 73

Table 5.2 Temperature dependent solid solubility of phosphorus and the sheet resistivity for silicon sample 75

Table 5.3 List of samples: n-type emitter formation on p type silicon substrate using APCVD thermal diffusion, spin on doping and dip coating by SOD solution 85

Table 5.4 Polarity measurement by using hot probe 86

Table 5.5 Doping uniformity measurement by hot probe 87

Table 5.6 Compositional analysis using EDS 90

Table 5.7 Measurement of sheet resistivity for doped sample using four point probe 92

Table 5.8 SiO_2 ARC film thickness measurement using spectroscopic reflectometer 93

Chapter VI

Table 6.1 Carrier generation and recombination for emitter, depletion and base layer 100

Table 6.2 Penetration depth and $1/V_{SPV}$ with respect to wavelength 104

Table 6.3 Carrier generation for emitter, depletion and base layer 106

Table 6.4 Carrier recombination for emitter, depletion and base layer 106

Table 6.5 Remaining carrier for emitter, depletion and base layer 107

Table 6.6 Data for reference cell 112

Table 6.7 Findings from in house fabricated mono-silicon solar cell (125×125 mm^2) 113

Nomenclature

APCVD- Atmospheric Pressure Chemical Vapor Deposition

ASH- Average Step Height

CVD- Chemical Vapor Deposition

DI- De-ionized

EDX- Energy dispersive x-ray spectroscopy

FE-SEM- Field Emission Scanning Electron Microscopes

HF- Hydro fluoric acid

IC- Integrated circuit

IPA- Isopropyl alcohol (Iso 2-propanol)

LIV- Light-current-voltage

PV- Photo voltaic

RCA- Radio Corporation America

SEM- Scanning electron microscopy

SOD- Spin on dopant

SPV- Surface photovoltage

SR- Spectroscopic Reflectometer

SRM- Spectral reflectance measurement

Chapter I

Introduction

1.1 Energy resources and consumption

The estimated maximum capacity for energy production given to all available resources on earth is called the world energy resources. The world's energy resources are divided into fossil fuel, nuclear energy and renewable energy [1]. Energy consumption refers to the amount of energy consumed in a process or by an organization or society. World energy consumption refers to the total energy used by all human civilization that is measured per year. The measurement involves all energy collect from every energy source and applied towards every single industrial and technological sector across every country [2].

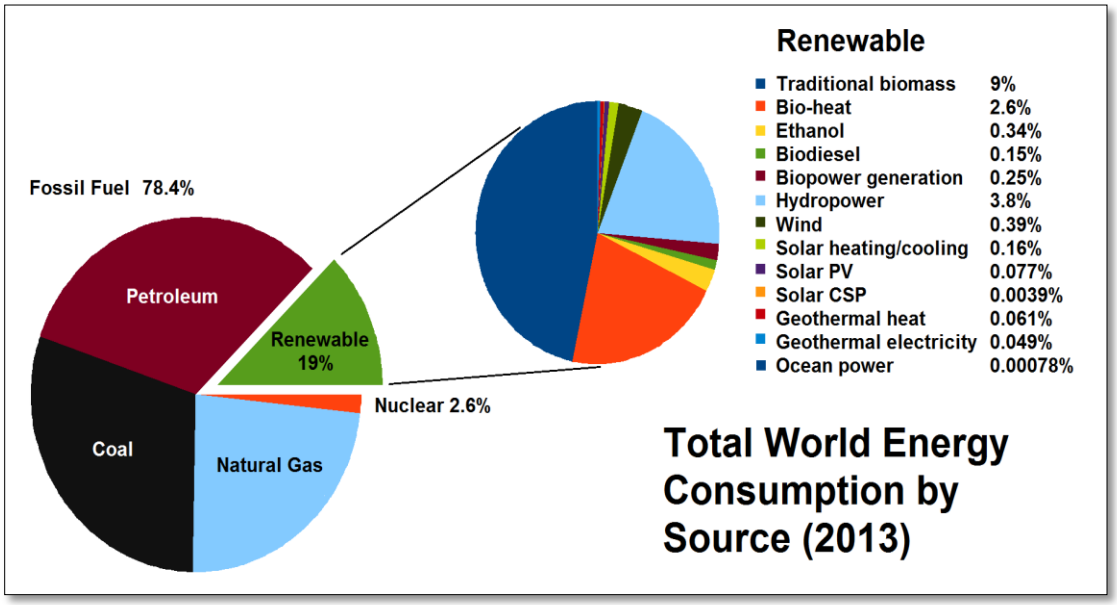

Figure 1.1 Global energy consumption at year 2013 [3]

Several institutions are involved to record and publish the energy data periodically. Some of them are U.S. International Energy Agency (IEA), the Energy Information Administration (EIA), the European Environment Agency etc [1].

1.1.1 Fossil fuel

The dominant energy resource from the early years is fossil fuel. The fossil fuel was supplying 86% of the world's energy at 2006 that is reduced with increasing years (source: US Energy Information Administration). Coal is the most burned and fastest growing fossil fuel because of its large reserves that make it popular to meet the energy demand of the global community. International Energy Agency said that the reserves of coal are 909 billion tones which could sustain the current production rate for 155 years. But at a 5% growth per annum the reserve would be reduced to 45 years or until 2051. The scenario of fossil fuel energy consumption in 1971 and 2013 is shown in figure 1.2 and 1.3 respectively (Source: IEA Statistics, OECD/IEA 2014).

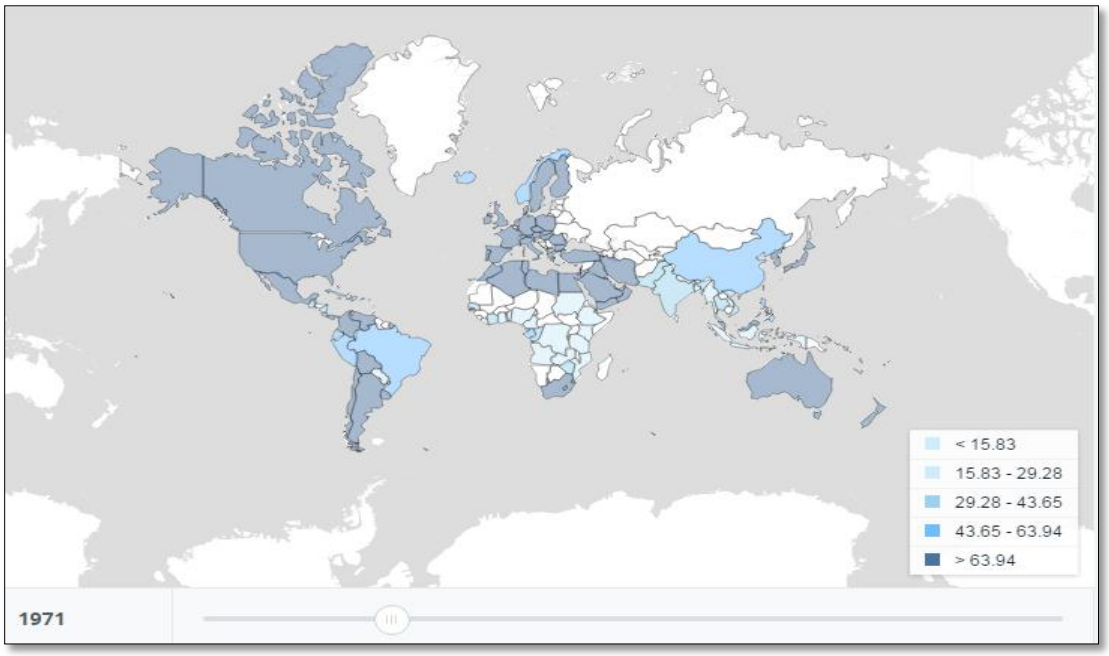

Figure 1.2 Fossil fuel energy consumption on 1971 (% of total) [4]

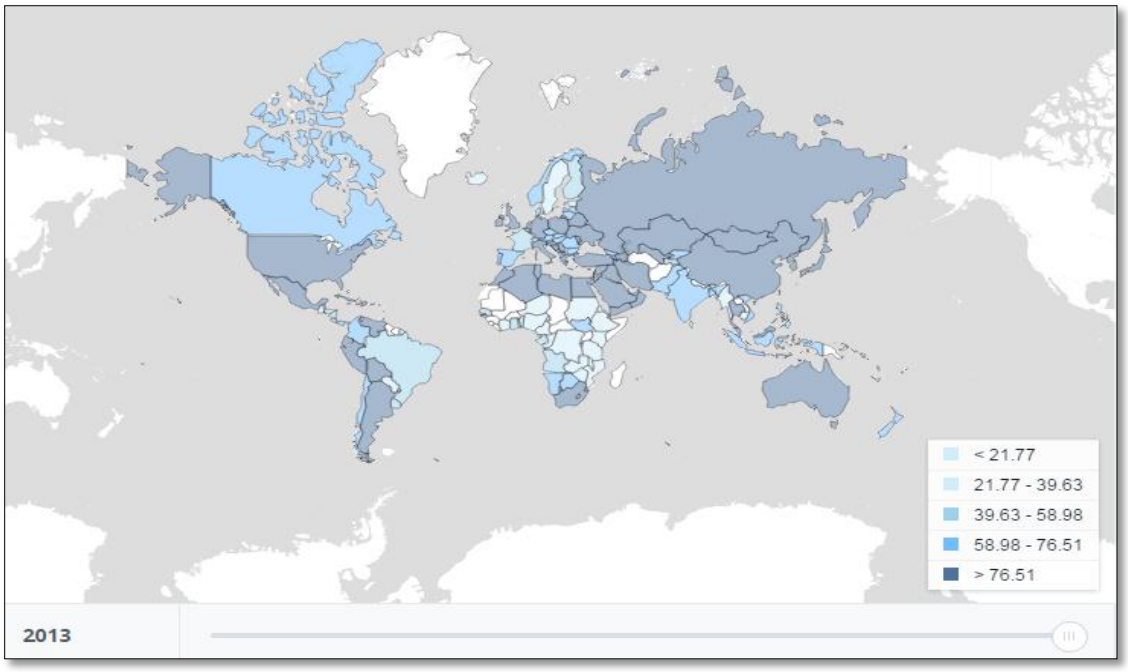

Figure 1.3 Fossil fuel energy consumption on 2013 (% of total) [5]

China is the example of coal fuel user in their industry that causes its polluted cities [6].Current oil consumption rate is 31.1 billion barrels (or 85-mbd).The peak oil production could be reached in the near future that will cause the severe oil price increases. According to peak oil theory, increasing production will lead to a more rapid collapse of production in the future, while decreasing production will lead to a slower decrease. OPEC had announced to decrease the production of oil by 2.2 mbd at the beginning of 1st January, 2009.The use of natural gas was 131% at 2009 compared to year 2000. North America shared 27% natural gas compared to other countries in 2010. The natural gas comes from European Union, North America, Latin America, Russia, Middle East, Asia, Africa etc [1].

1.1.2 Nuclear fuel

Due to a number of nuclear accidents the energy supply from nuclear fuel has restricted the growth at the end of last century. The world had 444 grid-electric nuclear power reactors with 62 others under construction in 2016.The commercial nuclear energy began in the mid 1950s. No new nuclear power plant was connected to the grid in 2008. But two were connected in 2009. The annual generation has been slight downward since 2007. According to IEA/OECD, Nuclear power met 11.7% of the world's electricity demand in 2011. The scenario of nuclear fuel energy

consumption in 2013 is shown in figure 1.4 (Source: IEA Statistics, OECD/IEA 2014).

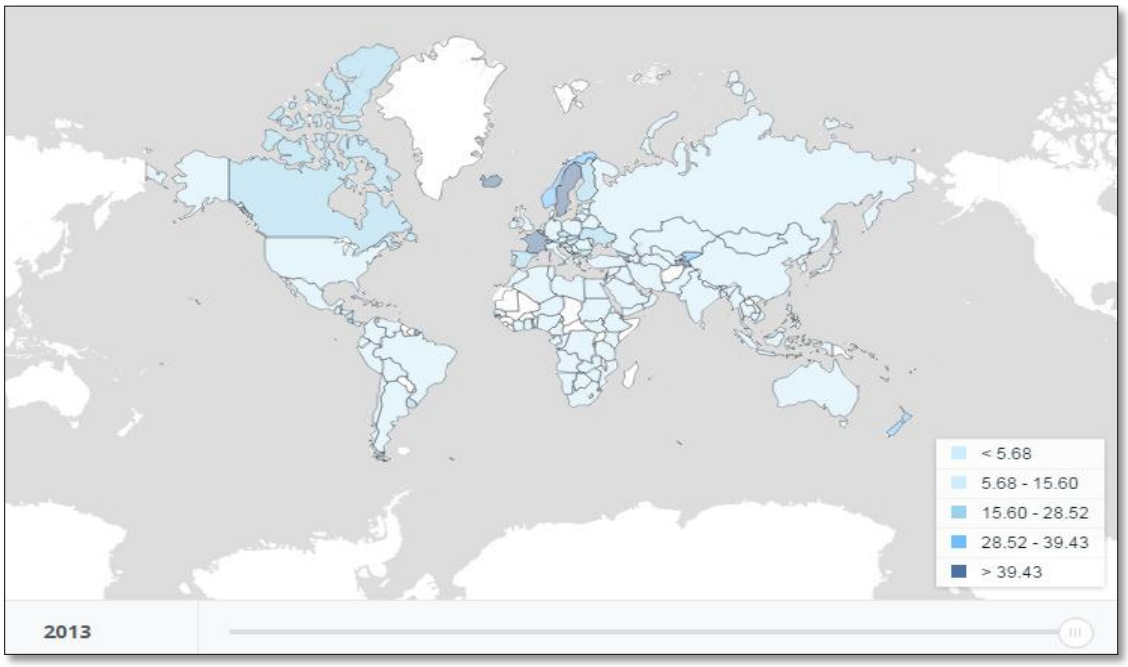

Figure 1.4 Alternative and nuclear energy (% of total energy use)[7]

Alternative energy production through hydrogen fusion has been started since 1950s.It generates large quantities of heat from the nuclei of hydrogen or helium isotopes. The heat can be used to generate electricity. Fusion is theoretically able to supply vast quantities of energy, with relatively little pollution.United States and the European Union, along with other countries are supporting fusion research [1].

1.1.3 Renewable energy

Day by day the world energy consumption is rising with the growth and development of the civilization. The primary solution of this increasing demand of using conventional energy source such as fossil fuel, nuclear power plant etc. it is now force to look into other renewable energy sources. Most of earth's available energy resources are renewable resources such as solar, wind, wave, tidal power etc.

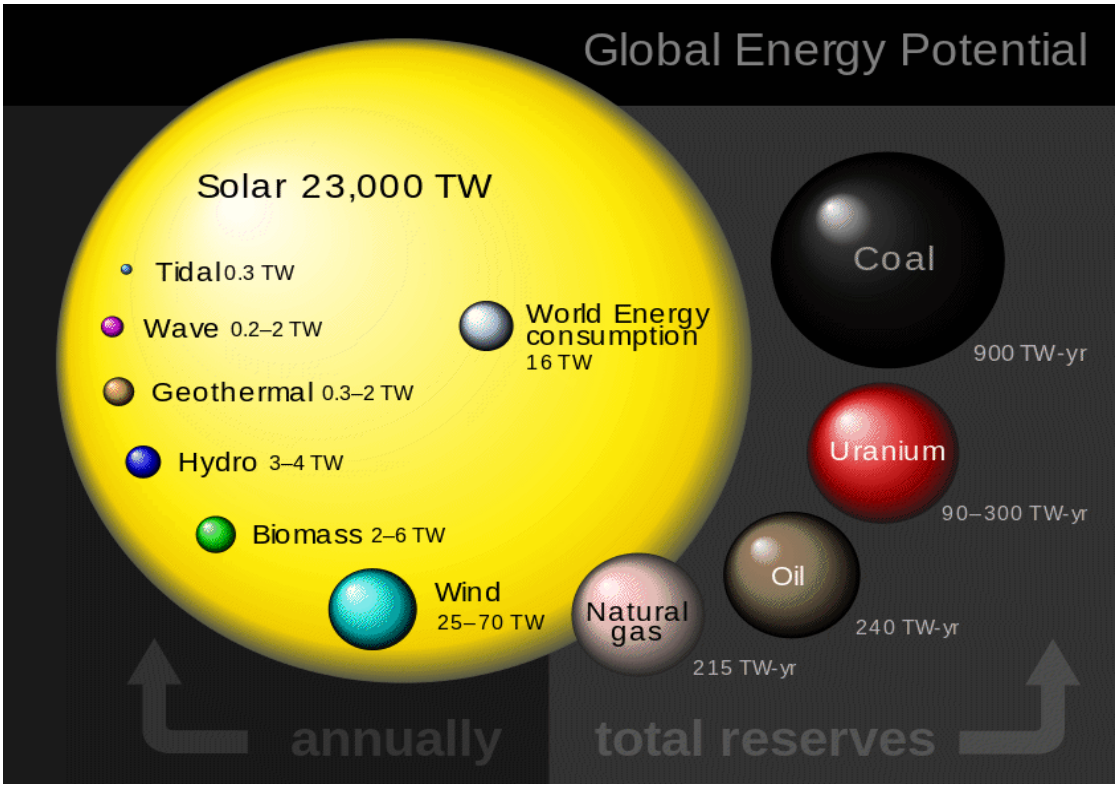

Figure 1.5 Renewable energy potential in 2009 [8]

Figure 1.5 clears that the renewable energy sources are larger than the fossil fuels.Theoretically they can supply the world's energy needs. The solar power that falls on the planet's surface is not possible to capture. Capturing less than 0.02% would be enough to meet the current energy needs. The annual average growth of solar generation was about 35% over the past few years. Japan, Europe, China, U.S. and India are the leading growing investors in solar energy.The drawback is that the current solar generation does not produce electricity at night in high northern and southern latitude countries.The energy demand is highest in winter while availability of solar energy is lowest. During these months the energy lacking could be overcome by buying power from countries closer to the equator. Alsothe technological developments such as the development of inexpensive energy storage can solve the energy crisis.

The estimated range of available wind energyis 300-870 TW (2005) [9]. Using the lower estimate, just 5% of the available wind energy would supply the current worldwide energy needs. The open oceans cover 71% of the planet and wind tends to blow more strongly there because of fewer obstructions.

The tidal forces created by the Moon and the Sun, and the Earth's relative rotation with respect to Moon and Sun. These tidal forces cause tidal fluctuations. Tidal fluctuations result in dissipation at an average rate of about 3.7 TW. At the end of 2005, 0.3 GW of electricity was produced by tidal force.Waves are derived from wind, which is in turn derived from solar energy, and at each conversion there is a drop of about two orders of magnitude in available energy [1].

1.2 Photovoltaic (PV) technology: Past and present

The development of photovoltaic began in 1839 when French physicist Edmond Becquerel discovered an increment in current of an electrolyte cell when exposed to light [10]. Nature published the effect of light on selenium during the passage of an electric current in 1873 that was described by British Engineer Willoughby Smith. An American inventor Charles Fritts first implemented the PV device of around 1% efficient in 1883. He had built up a junction by using selenium and thin layer of gold. Russian physicist AleksandrStoletov discovered the law of proportionality between the intensity of light and the corresponding photo induced current. He built the first solar cell based on the outer photoelectric effect and estimated the response time of the photoelectric current in 1888. Note that the outer photoelectric effect discovered by German physicist Heinrich RudlofHertzin in 1887. The Nobel laureate German born theoretical physicist Albert Einstein proposed a new quantum theory of light and explained the photoelectric effect in 1905. The p-n junction in CuO and silver sulphide photocells was described by Ukraine born Soviet experimental physicistVadimEvgenievichLashkaryov in 1941. An American Engineer Russell ShoemakerOhl hadpatented the Light sensitive device in 1946. He was a renowned
semiconductor researcher prior to the invention of the transistor[11]. In 1954 Bell laboratories scientist Gerald Pearson, Daryl Chapin and Calvin Fuller fabricated the first solar cell using silicon [12]. As the cost of commercial solar cell was as high as 300USD per watt it was not possible for mass production however it can be useful for powering satellites proposed by the mathematician from NewyorkGordon Raisbeck one of Daryl Chapin's colleague in 1955 [13]. Despite the initial concern of photovoltaic's future research continues and cost reduces to 100USD per watt by the year 1970 which was mainly used for powering satellites [14]. At present the

production cost reduces to <1 USD per watt peak for solar modules (≥ 125W) made of multi crystalline silicon [15]. Thus the number of terrestrial solar power unit's increases dramatically in various field of necessity of signaling, communication and remote sensing even powering the water pumps in agricultural fields. Now a days 99% of the terrestrial photovoltaic solar cells are made of silicon [15].

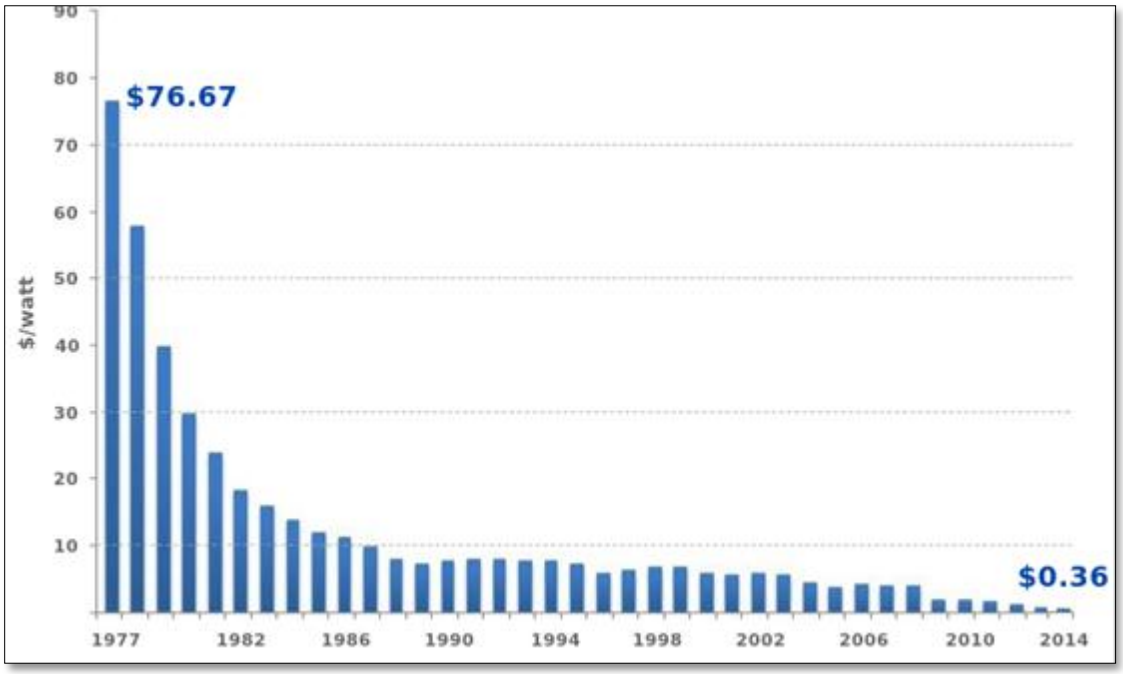

Figure 1.6 Price history of silicon PV cells in $ per watt [16]

1.3 Problem Statement

Since the inception of silicon based solar cells in 1954 by Bell lab researchers with a mere 6% conversion efficiency, the silicon wafer based cells experienced utmost achievement in terms of efficiency to its theoretical limit of around 25%, but still there are possibilities to achieve further improvement in efficiency to the Schokley Quissier limit. However, in terms of commercialization, cost is the most important issue to make it more popular as the competitors like CdTe thin film solar cells are quite comparable with silicon technologies. Therefore, there is a need to have cost reduction in silicon wafers, which is already achieved by thinning technologies as most common are now 180um, whereas initial wafers were over 500um. For mass production, cast silicon technologies are becoming fruitful to get us cheaper mono-crystalline silicon wafers. As many companies are developing cheaper silicon wafers and in case of any new comer in silicon wafer manufacturing, standard silicon solar cell processing may not be applicable. Moreover, there is a need for cheaper wafer

with simpler solar cell processing technology to be adopted to make silicon to hold the mainstream of solar cells in use for years to come. However, this sort of combination of raw materials and process should be investigated as most of the research groups are still focusing on higher effficiency issue, making tandem with newer materials like perovskite etc. We need to have more investigation on the characteristics for solar cells fabricated by the combination of cheaper raw materials and simpler process to get us the ultimate benefit from silicon technologies. Therefore, this study will mainly focus on the investigation related to characterization of silicon solar cells fabricated by commercially available low cost silicon wafer by simpler process.

1.4 Research Objectives

The main objective is to find out the correlation between the raw materials such as silicon wafer and the process options such as standard fabrication process for silicon monocrystalline solar cells. More precisely, It is to find out what could be the various characteristics such as optical, structural and electrical characteristics of the low-cost commercially available thinner silicon wafers in case processed by simplied process of fabrication in a pilot experimental facility. Therefore, this study embarks on the following specific objectives as shown below:

1. To investigate a simplified solar cell fabrication process for commercially available thinner mono crystalline silicon wafer to improve overall cost-efficiency.
2. To Explore the standard processes of Emitter Formation, Surface Passivation and Enhanced Light Trapping in case of Thinner silicon wafers.
3. To Examine the properties, such as optical, structural and electrical, of the processed wafers by low-cost characterization tools and techniques for process optimization and cost-efficiency.

1.5 Materials for Photovoltaics

Since only photons with energies above the band gap of a semiconductor are absorbed, the band gap of the material used for a photovoltaic device must be engineered in order to produce the maximum power for a given illumination, given

that the solar spectrum as a function of photon energy under one sun condition [18, 19]. Semiconductors with larger band gaps produce higher photovoltages, but absorb and convert fewer of the incident photons, resulting in lower currents. Semiconductors with smaller band gaps absorb most of the solar radiation, but convert most of the energy to heat. A balanced condition for the solar cell with the best efficiency is to use material with band gap near the peak of the solar spectrum, between 1 and 2 eV[20].

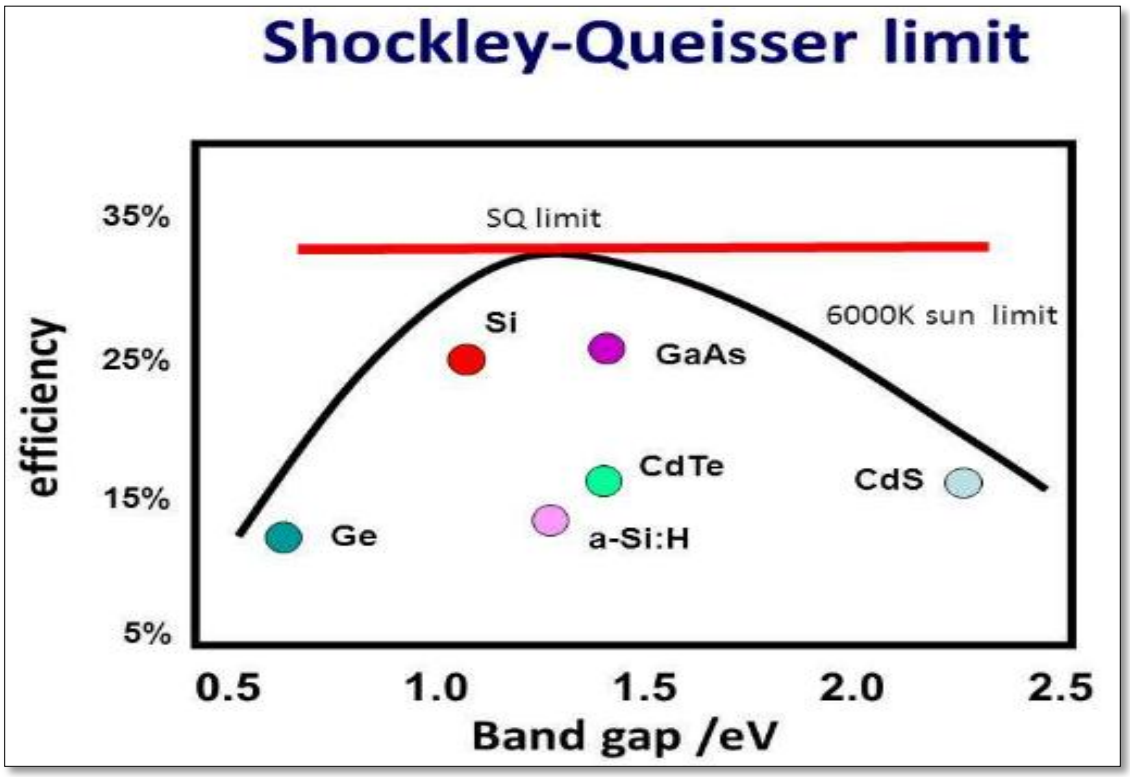

Figure 1.7Bandgap and efficiencies for photovoltaic materials[21]

Compound semiconductors GaAs, GaInP, InP, CdTe, and CIS (copper indium diselenide), and indirect band gap materials, like silicon, are used in the fabrication of solar cells. Both amorphous and crystalline (polycrystalline and monocrystalline) silicon are used in the manufacture of photovoltaic devices. However, amorphous silicon suffers from the Staebler-Wronski effect [22], in which dangling bonds are created under illumination, causing the efficiency to degrade. Research communities turn then to crystalline silicon technology, which is capable of providing efficiencies greater than 20% [23]. Material bandgap and related efficiencies is shown in figure 1.7 (Source: DOE, Lewis Group at Caltech).

1.6 Mono-crystalline silicon technology

One of the most promising technologies for reduced cost photovoltaic technology involves the reduced thickness mono-crystalline silicon wafer or substrate. The efficiencies of mono-crystalline silicon solar cells have much higher efficiencies than thin-film polycrystalline solar cells. Although production costs are significantly lower for thin film polycrystalline solar cells than the mono-crystalline silicon cells.In 2014 the conversion efficiency of mono-crystalline silicon solar cell reached to 25.6% at research level. Panasonic HIT® solar cells achieved that efficiency with cell area 143.7 cm^2. The previous record was 24.7% with cell area 100 cm^2 in 2013 [24].

Generally silicon wafers produce from Czochralski (CZ) process. Most of the PV industries today use the mono-crystalline silicon wafers. Because the mono-crystalline silicon wafers have lower defects compared to other wafers. The solar cells produce from this type of wafer has maximized the power density in the PV module and to reduce the cost per unit energy.The wafers are classified in accordance with their crystal orientation, doping type, resistivity, thickness, concentration of oxygen and carbon etc. Today's commercial wafers are of pseudo square shaped (cylinders are shaped as squares with rounded off corners) geometry. Crystal orientation has strong influence on the optical and electrical performance on solar cells. The etching rate of mono-crystalline <100> crystal orientation is higher than the <111>which helps for early growth of pyramids.The wafer size and thickness depends on the ability to handle during cell processing. To reduce the material cost, the wafers are cut into 120-200 μm thickness with multi-wire sawing. Thinner wafer reduce the material consumption may require requires an automated handling process fabrication. Decrease the wafer thickness means increases the possibilities of breaking wafers. Most of industrial solar cells are based on boron doped p-type wafers and n-type diffused emitter. N-type wafer price is still now much higher than p-type. N-type wafer shows large minority carrier diffusion length and carrier lifetime than the p-type wafer [25].

Table 1.1Properties of silicon [26, 27]

Property		Value
Basic parameter at 300 K	Crystal structure	Face centered diamond-cubic
	Number of atoms in per cm^3	5×10^{22} cm^{-3}
	Density (ρ)	2.328 gcm^{-3}
	Dielectric constant	11.7
	Lattice Constant	5.431 Å
Band structure and carrier concentration	Energy Bandgap (EG)	1.12 eV (at 300 K)
	Intrinsic Carrier Concentration (ni)	$1 \times 10^{10} cm^{-3}$ (at 300 K)
Electrical properties	Electron mobility	$\leq$1400 cm^2 $V^{-1}s^{-1}$
	Hole mobility	$\leq$450 cm^2 $V^{-1}s^{-1}$
	Diffusion coefficient of electron	$\leq$36 cm^2/s
	Diffusion coefficient of hole	$\leq$12 cm^2/s
Optical properties	Absorption Coefficient α_n	$10^{-18}.n_0.\lambda^2$ (at 300 K, $\lambda \geq 5\mu m$)
Thermal properties	Melting Point	1412 °C
	Thermal Conductivity	149 $W.m^{-1}.K^{-1}$
	Thermal diffusivity	0.8 cm^2/s
	Thermal Expansion Coefficient	$2.6 \times 10^{-6} K^{-1}$

1.7 Principle of solar cell operation

A solar cell is a simple device: just a p-n junction with light shining on it. To maximize efficiency we need to maximize the generation of e-h pairs and minimize the recombination of e-h pairs. For the case of p-n junction diode under dark condition: anytime an electron and hole recombine anywhere within the diode, one electron flows in the external circuit. . For the case of p-n junction diode under light: anytime an electron and hole pairis generated within the diode, one electron flows in the external circuit [28].

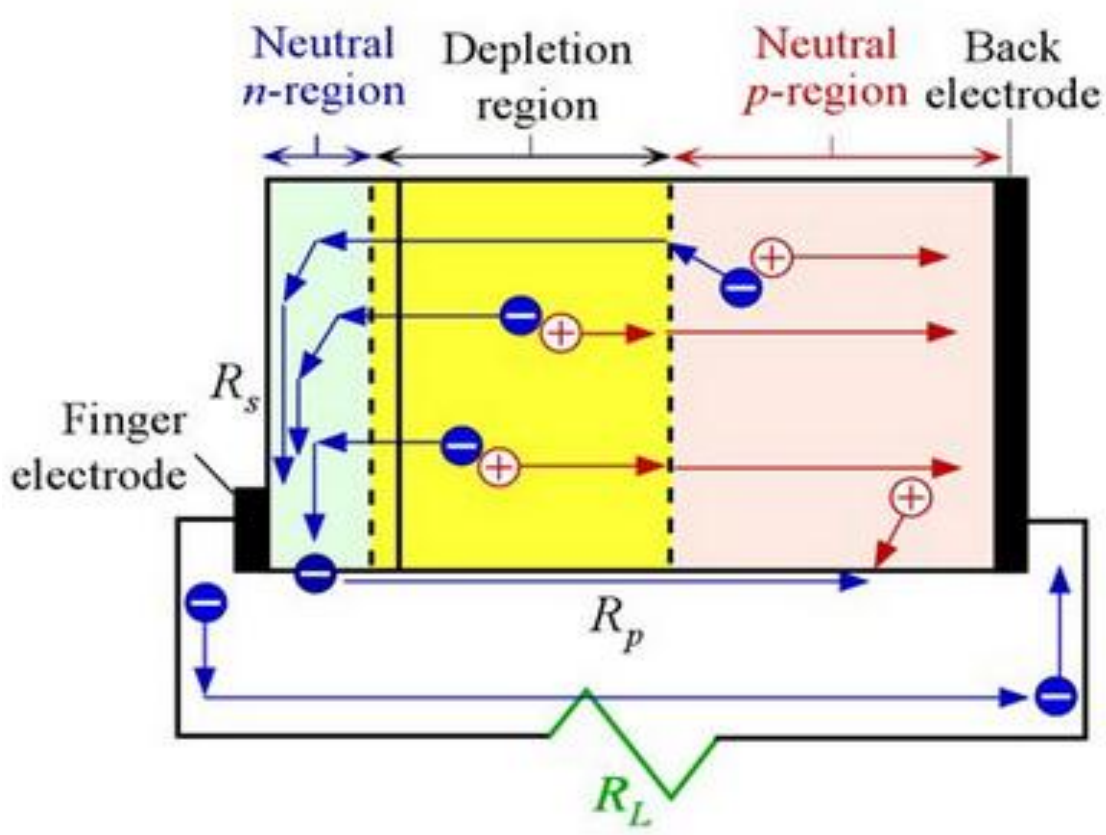

Figure 1.8 Working principle of solar cell

1.8 Efficiency of silicon solar cell

Solar cell efficiency refers to the portion of sunlight energy that can be converted into electricity via photovoltaic. Since January 1993, Progress in Photovoltaic has published six monthly listings of the highest confirmed efficiencies for a range of photovoltaic cell and module technologies [29, 30, 31]. Here mentioned results up to 2014, published in the solar cell efficiency table (version 44) [32] shown in table 1.2.

Table 1.2 Highest confirmed terrestrial solar cell efficiency measured under AM1.5 spectrum

Classification of solar cell	Efficiency (%)	Description	References
Silicon (Crystalline)	25.6±0.5	Panasonic (HIT structure)	[33]
Silicon (Multi crystalline)	20.4±0.5	FhG-ISE	[34]
Silicon (amorphous)	10.1±0.3	Oerlikon Solar Lab, Neuchatel	[35]
Silicon (Micro crystalline)	11.0±0.3	AIST	[36]
Si (large multi crystalline)	19.5 ± 0.4	Q-Cells, laser-fired contacts	[37]
III-V GaAs Thin film	28.8±0.9	Alta device	[38]
CIGS thin film cell	20.5±0.6	Solibro, on glass	[39]
Dye sensitised cell	11.9±0.4	Sharp	[40]
Silicon (mini module)	10.5±0.3	CSG solar (<2μm on glass, 20 cells)	[41]

1.9 Review of Literature

The foundation for PV device operation and improvements was formulated in the period from 1905 to 1950. The key events in this period were Einstein's photon theory, Czochralski crystal growth method for single crystal silicon and germanium growth and the development of band theory for high purity single crystal semiconductors [42, 43, 44, 45].

In 1940, Russell Shoemaker Ohl, researcher at Bell Laboratory noticed that current had flown in a particular cracked silicon sample when it was exposed to light. Ohl had inadvertently made a p-n junction and the crack probably formed between the boundary of p and n region. Ohl patented (US Patent 2402662, "Light sensitive device") his solar cell in 1946, which was about one percent efficient [46].

The first practical single crystal silicon solar cell was created in 1954 at Bell Laboratories by Pearson, Chapin, and Fuller. They faced the problem of making good electrical contact and the impurity material. Later they solve those problems and made

boron-arsenic silicon sells. Those first silicon solar cells were about 6 percent efficient. Pearson, Chapin, and Fuller had patented (patent US2780765, "Solar Energy Converting Apparatus) their solar cell in 1957, which was about eight percent efficient [47, 48].

First applications of PV solar cells were on space satellites, later for initial terrestrial applications. First Telstar communication satellite launched in 1962 which was powered by silicon solar cells is shown in figure 1.9[49]. In 1970s, silicon cells were evolved for use in terrestrial installations. The foundation was then laid for the development of a variety of markets for PV solar cells.

Figure 1.9Telstar communication satellite [50]

The international participation in PV cell deployment from 2000 to present was shifted from US to Germany, China, and Japan. German Renewable Energy Sources Act creates a Solar Feed-In-Tariff (FIT) which creates a solar market in Europe [51]. Suntech Power is then formed in China in 2001 [52]. In 2011, fast-growing factories in China push manufacturing costs down to about $1.25 per watt for silicon photovoltaic modules [53].

The standard industrial solar cell production is mainly carried out on boron doped mono-crystalline or Cz Si wafers in 1951 [54]. The thinner wafer of 150 to200 μm is introduced with active cell area of 125x125 mm^2 or 156x156 mm^2 in 2010 [55]. Industrial processing steps are- the saw damage etching, both side texturing by wet

chemical etching, phosphorous emitter diffusion by $POCl_3$, HF cleaning, the edge isolation, the front surface iscoated with SiN_x:H anti-reflection and passivation layer, contact formation by screen printing where silver (Ag) containing front contact and the rear side is typically fully covered by an aluminium (Al) based paste [56]. Note that SiN_x:H film is an excellent surface passivator and a very good AR coating material. Whereas SiO_2 film is an excellent surface passivator and AR coating performances is slightly lower compared to SiN_x:H film; the overall performance is good [57]. The wafers then go through co-firing step, where the front contact paste etches through the SiN_x:H layer and establishes contact to the emitter. Simultaneously on the rear side the Aluminium BackSurface Field (Al-BSF) is formed. Additionally, the hydrogen-rich SiN_x layer releases hydrogen during the firing step which can passivate defects in the Si crystal. The efficiencies obtained with this type of process in industry today are up to 19.2% for mono (Cz) Si wafers (including a selective emitter structure)[58]. In average, efficiencies above 17% for standard mc Si and above 18% for Cz Si are possible [59].

At present, in order to reduce cost, various researches are ongoing for the improvement of fabrication and characterization process for commercial solar cell production. In 2010, Vikram*et al.*at the University of Virginia,reported a simplified single step process for Cz and Fz- substrate of c-Si photovoltaic device fabrication. Single step incorporates the thin film of phosphorus doped spin on dopant (SOD) serves as dopant source, anti-reflection coating (ARC) and a surface passivation layer. They have reported the conversion efficiency of over 15% [60].

Plasma Enhanced Chemical Vapor Deposition (PECVD) equipment is widely used in SiNx:H film surface passivation and ARC coating in the industrial fabrication process. But the concept of simplified fabrication process gives the idea of SiO_2 film as surface passivator and ARC on mc-silicon solar cells [60]. This will helps to avoid costly equipment PECVD, avoid the using HF, and reduce the processing steps as well as process monitor steps. Less production cost can be hearten and accelerated the expansion of production into radical levels. Moreover, the toxic silane gas can be avoided which gives rise the environment friendly fabrication.

The measurements on solar cell wafers yield unreliable values for commercial aspects. Hence, in most cases, the solar cell industry uses additional “control wafers (dummy)” in each process step that are polished on one side. Another important issue is measurements are made on small areas. In solar cell monitoring, it is important that

the properties of the entire wafer be measured because of non-uniformities. Most of the cases the measurement equipments are expensive [61]. The major process steps, parameters are monitored by different techniques. The list of the major process steps, parameters that are monitored are given in the following table 1.3.

Table 1.3 Major process steps, parameters and the monitoring techniques used in solar cell fabrication [61]

Process or monitor step	Parameters	Technique
Crystal growth (ingot quality)	τ	PCD
Wafer cleanliness	Surface roughness	Reflecteance
Texturing	Texture height	SEM/ Optical microscopy/ Reflectance
Electronic quality of wafer	L/τ	SPV/ PCD
Junction depth	Sheet resistance	4 point probe/ groove and stain
Defect Density	Dislocation Density	Chemical Delineation / TEM
Impurity Concentration		FTIR, NAA, SPV, DLTS
AR-Coating	Thickness, Refraction Index	Ellipsometer/Interference
Metallization	Line Width	Optical/SEM
I-V of Cell	Voc, Jsc, FF	Standard I-V measurement

1.10 Organization of thesis

This thesis is organized first with a brief introduction into the photovoltaics history, its market potential and the current status of commercialmono-crystalline silicon solar cell in photovoltaic industry.Chapter 2 is a summary of theory and instrumentation techniques of characterization tool. Chapter 3 follows the characterization of the silicon wafers such as type measurement, thickness measurement, physical and sheet resistance measurement etc. This chapter also discussed about the low cost in-house made hot probe technique and took some characteristic curves from this tool. It also covers the carrier concentration changes inside the wafers due to thermal effect. Chapter 4 follows the properties of isotropic and anisotropic etched samples. It follows the p-type etched silicon samples thickness measurement, 2D optical microscopy, SEM imaging, stylus surface profiling for structural characterization, optical characterization through spectroscopic reflectometer and SRM. Chapter 5 is a summary of atmospheric pressure chemical

vapour deposition (APCVD) diffusion process with single step for doping and surface passivation and ARC. Spin on doping is also discussed here.It follows the properties of phosphorus doped emitter layer on the boron doped silicon wafer. It covers the polarity measurement, doping uniformity measurement, SEM imaging, compositional analysis by EDS, optical reflectance measurement, sheet resistance measurement and ARC film thickness measurement. Chapter 6 discusses the surface photovoltage measurement. It covers the measurements of minority carrier diffusion length, minority carrier lifetime, carrier generation and recombination inside the three regions of solar cell. It also discusses the conversion efficiency measurement technique. It covers the measurements of open circuit voltage, short circuit current, fill factor, efficiency, maximum voltage, maximum current and maximum power.

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Chapter II

Characterization Techniques

2.1 Introduction

This chapter briefly describes the characterization techniques used to study the properties of p-type and n-type silicon for photovoltaic application. Methodology and theoretical aspects related to morphological, structural, optical, and electrical characterization techniques are discussed. Brief discussion on energy dispersive x-ray spectrography for compositional analysis, surface photo voltage near infrared spectroscopy is also presented. Brief descriptions of instrumentation setup are also explained in this chapter.

2.2 Measurement of thickness

Dial indicator measures the thicknesses of thin sample with the gauge less than 1.5 N pressures on the sample substrate and provide lowest friction for smooth and precise operation. Dial indicator of model no- 2110S-10, Mitutoyo, Japan for measuring the micron range thickness of the silicon samples was used in this research. The instrument uses stem-bush design for trouble-free stem clamping. For smooth movement of spindle into the stem there is involutes curved lifting lever. The stem is made of high-strength quench-hardened stainless steel which resists arduous use. Dial Indicator lug back range 0.001mm or 1 μm and the indicator uses jeweled bearings providing excellent indication sensitivity and durability. The smaller indicator indicates the number of rotation of the larger indicator to complete its full cycle. The accuracy of this instrument is ±5 μm [1].

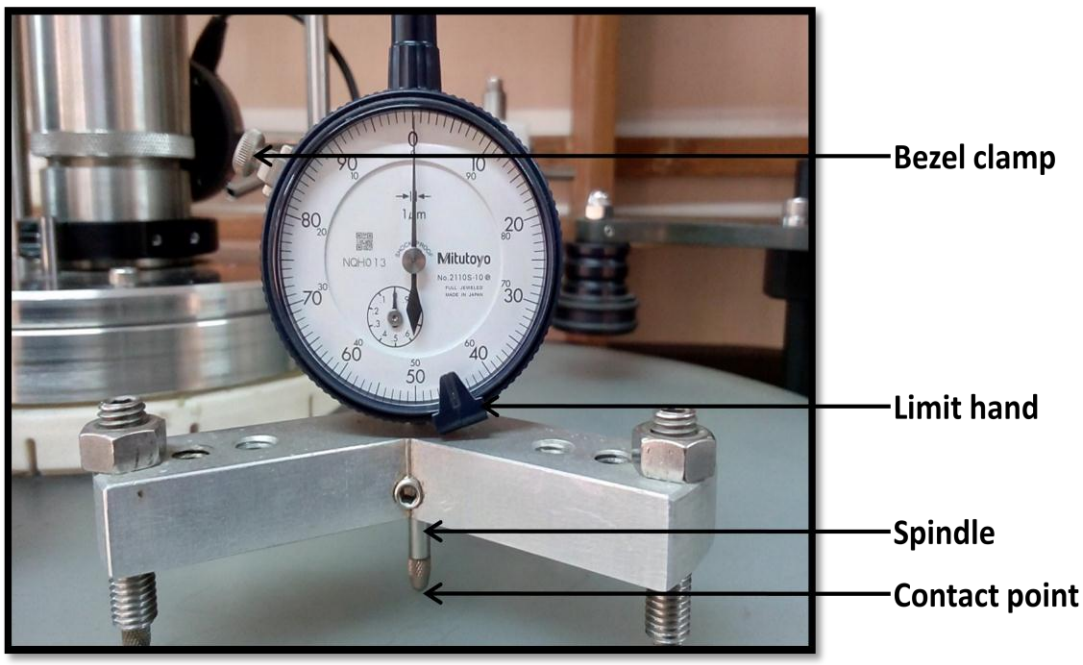


Figure 2.1 Front view of dial indicator

2.3 Optical reflectance

2.3.1 Spectroscopic reflectometer

Spectroscopic reflectance measures the amount of light reflected from the surface of a thin film over a range of wavelengths with the incident light perpendicular to the sample surface by which one can use for measuring the thickness of a thin transparent and semi-transparent film [2]. Spectroscopic reflectometer was supplied by Radiation tech. company ltd. (Taiwan). It measures not only the thickness of oxide layer on the doped silicon surface but also the reflectance pattern over a range of wavelengths (380-1000 nm) for various stages of sample preparation. The instrument uses optical techniques to determine thin film characteristics by measuring how the film interacts with white light. Before measuring the thin film characteristics the instrument was calibrated using a reference sample that contains a thin film layer of SiO_2 on SiCr substrate.

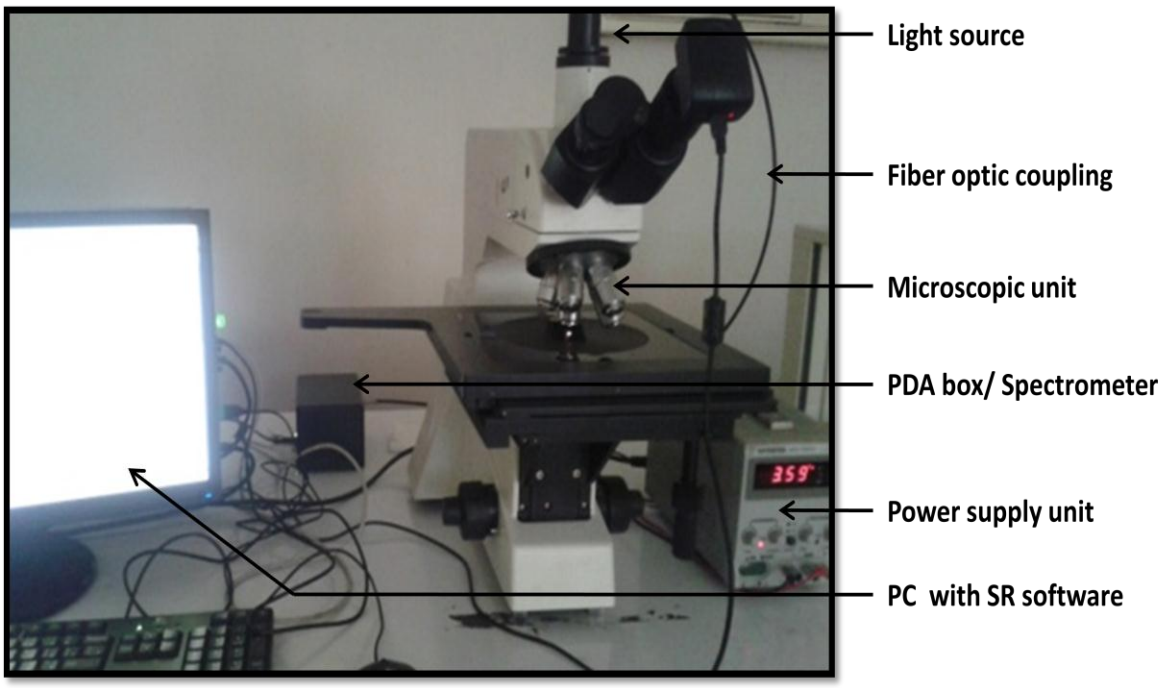


Figure 2.2 Front view of spectroscopic reflectometer

Reflectance (R) is defined by [3]

$$R = \frac{I_{refl}}{I_{inc}} - - - - - - - - - - - - - (2.1)$$

Here I_{inc} is the incident light intensity, I_{refl} is the reflected light intensity.

The instrument only measures the reflected light intensity (I_{refl}). To determine the reflectance (R) the instrument needs to know the value of incident light intensity (I_{inc}). So initially a reference sample (TRF 008) with a known reflectance (R_0) is measured by the following expression

$$R_0 = \frac{I_{r0}}{I_{inc}} - - - - - - - - - - - - - (2.2)$$

Here R_0 is the reflectance of reference sample and I_{r0} is the reflected light intensity of the reference sample.

The reflected light has been analyzed from the sample by passing it through a spectrometer. A microscope attached with this tool to shine small area of the sample [4]. The light detection performed using photo diode array with the various wavelengths falling in the different diodes in the array for automatic data acquisition.

Film properties are determined by calculating reflectance spectra based on varying trial values of thickness and the n (refractive index) and k (extinct constant) model parameters until the calculated reflectance matches the measured reflectance best and that is called Best-Fit-Algorithm [3].

2.3.2 Spectral reflectance measurement (SRM)

SRM was used to measure the light reflection from initial stage to textured stage and then compare to the reflectance of standard mirror and then calculate the percentage of reflectivity over a spectral range of 400-1200 nm. This instrument is established in Solar Cell Fabrication Laboratory, Institute of Electronics, Atomic Energy Research Establishment, Savar, Dhaka.

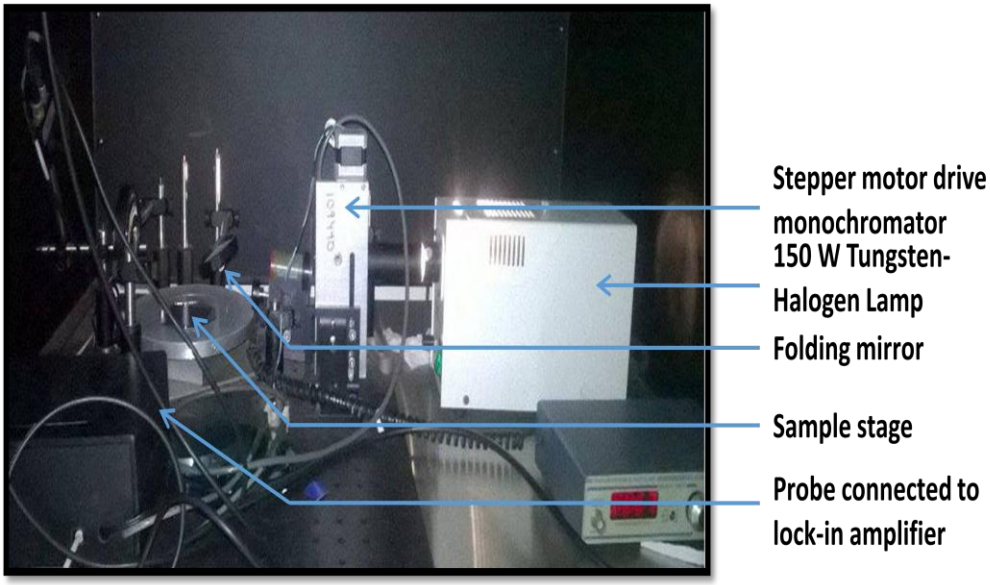


Figure 2.3 Front view of surface reflectance measurement

2.4 Surface Morphology

Surface morphology includes the quantitative evaluation of features, size, shape of silicon substrate etc.

2.4.1 Scanning Electron Microscopy (SEM)

Topographical observation of silicon sample was taken out using Field Emission Scanning Electron Microscopes (FE-SEM) from Zeiss Sigma series with EDX system [5]. In conventional SEM thermionic emitters uses electrical current to heat up a tungsten or lanthanum hexa boride (LaB_6) filament. When the heat is enough to overcome the work function of the filament material, the electrons can escape from the material itself. Thermionic sources have relative low brightness,

evaporation of cathode material and thermal drift during operation. Here Field Emission is one way of generating electrons that avoids these problems. A field emission (FEG) does not heat the filament. The emission is reached by placing the filament in a huge electrical potential gradient. The FEG is usually a wire of Tungsten (W) fashioned into a sharp point. The image in an SEM is produced by scanning the sample with a focused electron beam and detecting the secondary or backscattered electron most commonly with an Everhart-Thornley (ET) detector [6].

Figure 2.4 Front view of Scanning electron microscope

Images were taken with 5kV electron beam, close working distance 8.1 mm and normal incident electron beam on the sample surface.

2.4.2 2D optical microscopy

An optical microscope by Radiation tech. company ltd. (Taiwan) was used for optical imaging as a primary tool for viewing surface morphology of raw, cleaned, textured and diffused silicon wafer.

Optical 2D image of silicon film was taken using bright field microscopy where light falls vertically on the top surface of the sample. Bright field microscopy is useful to observe the sample surface topography.

$$s = \frac{0.61\lambda}{NA} - - - - - - - - - - - - - - (2.3)$$

Resolution (s) of image can be calculated using equation (2.3) where NA=1, λ=633 nm which gives resolution s= 386 nm [7].

2.5 Surface roughness measurement by Stylus surface profiler

The measurement carried out for surface roughness of samples by stylus surface profiler. Dektak 150 stylus profiler from Veeco was used for measuring the four sided pyramid height of textured silicon sample. From this measurement one can find out surface roughness with standard scan of hills and valley profile with the stylus force of 3 mg and 56 nm resolutions [8, 9].

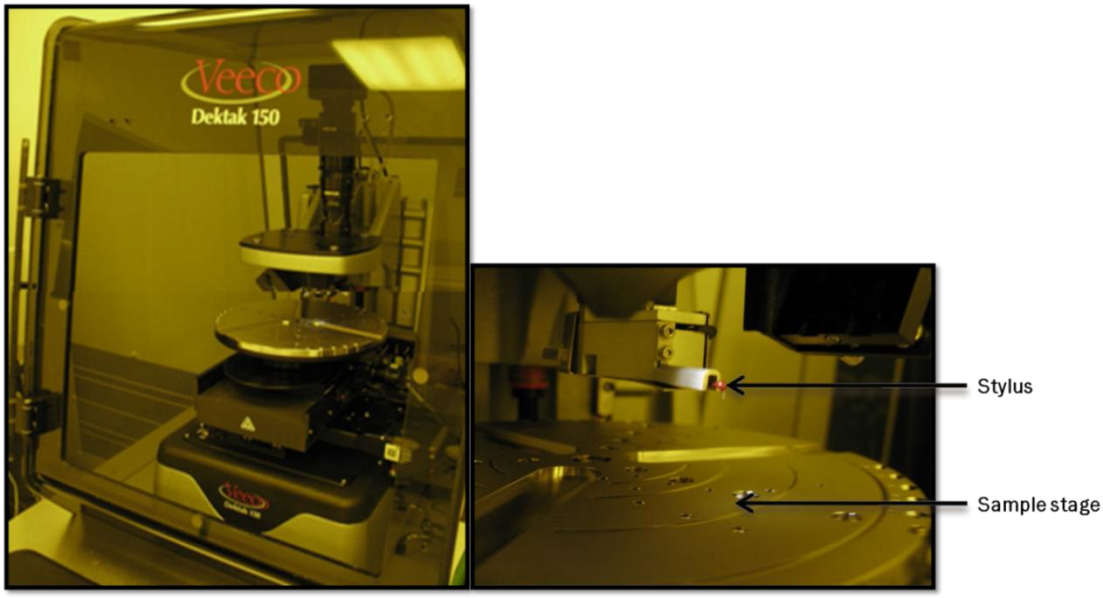


Figure 2.5 (a) Front view of dektak stylus surface profiler (b)) Close view of stylus tip

The profiler incorporates an optical deflection height measurement mechanism and magneto static force control system which results in a low force (0.03-15 mg) and low inertia stylus assembly. This makes the surface profiler capable of measuring soft films and substrates without surface damage. In this case we allowed the stylus to exhibit a very low force on the sample surface as 3 mg that's why the sample left scratch free after the measurement [8, 9].

2.6 Compositional analysis by energy dispersive x-ray (EDX) spectroscopy

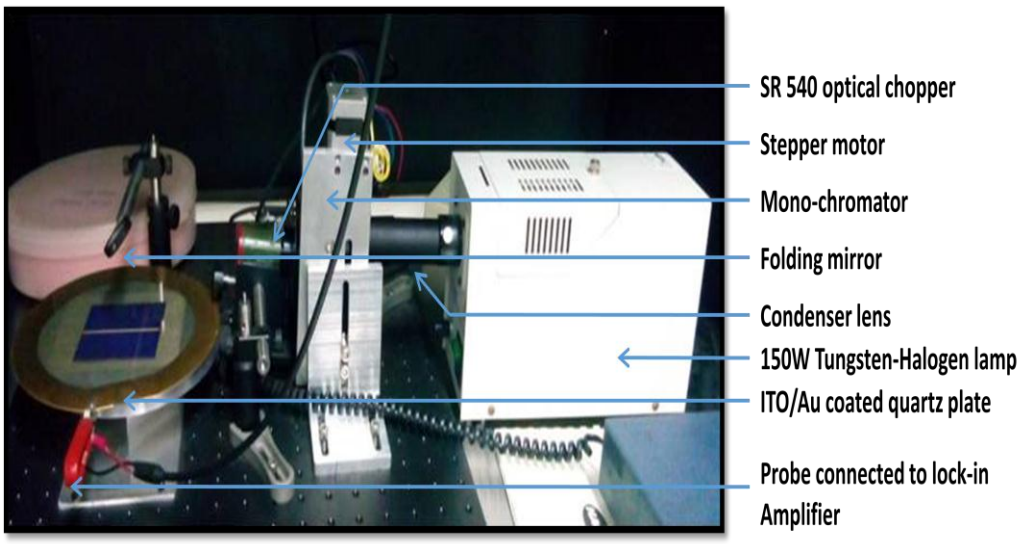
Electron microprobe method first described in 1948 [10]. The method consists of interaction of electron with inner shell electrons. This bombardment of electron cause ejection of electrons from one of the inner atomic shell and allows electrons from higher atomic shell dropping into the vacancies created by the ejected electrons. If the X-ray emission is the result of an L to K shell transition, the X-rays are known as Kα, If the X-ray emission is the result of an M to L shell transition, the X-rays are known as Lα and so on [11, 12].

The emitted X-ray from the sample have energies characteristic of the element from which they originate, leading to elemental identification. An appropriate X-ray detector can be used to detect the characteristic X-ray spectrum from the sample [13]. Elemental identification can be performed by matching the experimental spectrum to known X-ray energies which is automatically done using appropriated software.

In this study FE-SEM from Zeiss Sigma series with EDX system with 10 mm silicon drift X-ray detector (SDD) for compositional analysis of doped silicon sample has been used [5, 6]. An electron beam of 20 keV as excitation source has used. Intensity versus photon energy curve allows us to evaluate the elemental analysis of impurity doped silicon substrate. It has detected silicon, phosphorous, presence of oxide layer on silicon using EDX spectrum. Peak position are analysed corresponding to O is 525 eV (Kα), Si is 1.739 KeV (Kα), P is 2.013 keV (Kα) [14,15].

2.7 Optical properties: Surface Photo Voltage Spectroscopy

Spectrometer is an instrument which is consists of a monochromator in between the light source and the sample, ensuring that only selected wavelengths are incident on the sample at one time. Monochromator is used to separate white light into its spectral components for a subsequent spectral response measurement. Using appropriate size of slit one can vary the illumination area on the sample. Light directed on the sample by using a folding mirror. The contact probe collects the signal and fed into the lock in amplifier. A chopper provide reference signal to the lock in amplifier to ensure all the stray light are rejected by the system (electrical noise canceller) and enhance system sensitivity from nV to mV range [16, 17].



(a)

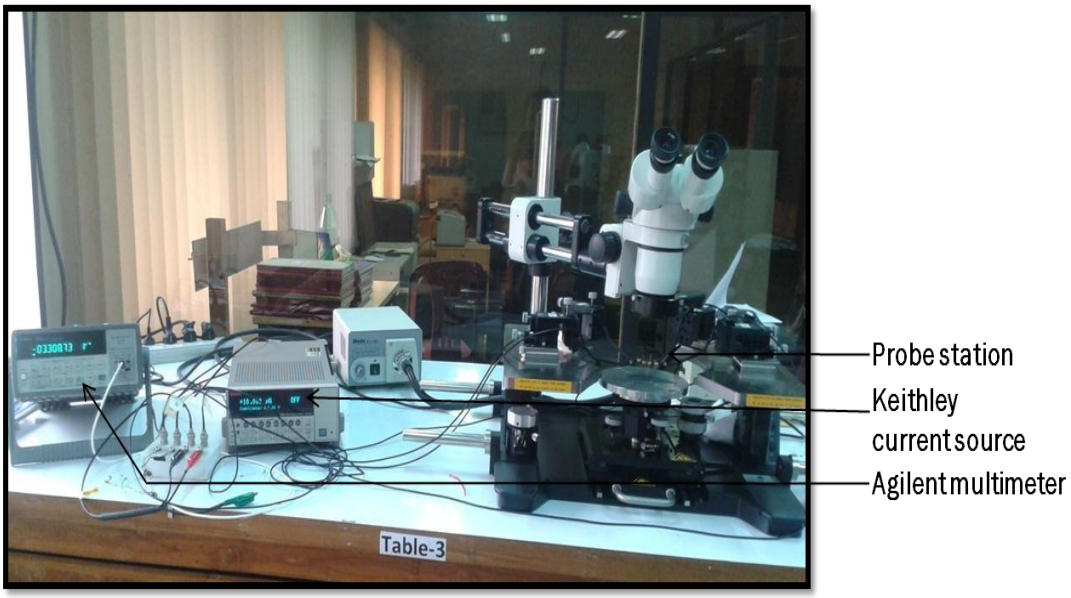
(b)

Figure 2.6 (a) Front view of SPV spectroscopy (b)) Front view of stanford research 510 lock-in amplifier

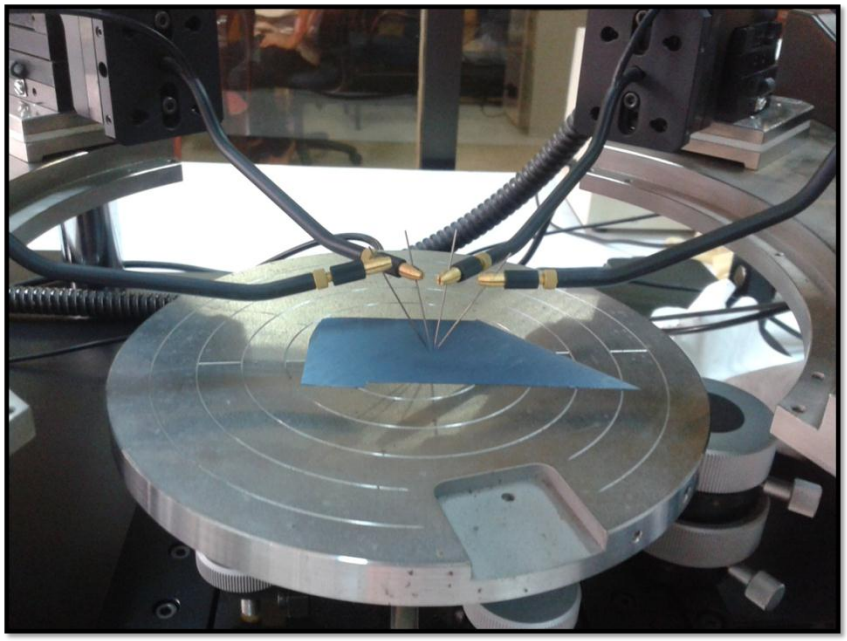
In this study, a spectrometer has used that was capable of recording spectra in the visible range as well as in the near infrared (400 nm to 1200 nm). The system consists of 150W tungsten halogen fibre optic microscopic illuminator, stepper motor driven monochromator, phase-insensitive Stanford research 510 lock-in amplifier, chopper, Aurum coated wafer chunk, ITO/Au coated quartz plate, vacuum pump, contact probe, folding mirror, LIV software for data acquisition. The Lab-view interface produce wavelength vs surface photo-voltage graph. Note that surface photovoltage is the electrochemical potential changes on the silicon sample surface due to illumination.

2.8 Electrical properties measurement by four point probe

Four point probe setup is commonly used to measure resistivity of semiconductor film as the arrangement eliminated the resistance from wire and contacts. Resistivity calculation for silicon sample using four point probe can be explained with the following equations [18].



(a)



(b)

Figure 2.7 (a) Four point probe (b)) Close view of four point probe

$$\rho = 2\pi sF\frac{V}{I} - - - - - - - - (2.4)$$

Here, s is equal probe spacing, F is correction factor which depends on sample thickness, diameter, temperature, V is voltage and I is current.

$$\rho = 4.532\ t\ \frac{V}{I} - - - - - - (2.5)$$

Here, t is sample thickness.

Sheet resistivity can be calculated from

$$R_{sh} = 4.532\frac{V}{I} - - - - - - - - (2.6)$$

In this study, a four point probes set up was used by using a probe station of Cascade Microtech, D-01561 Sacka, Germany. Probe spacing was maintained 1 mm each. A MLC 150C probe station illuminator was used for the purpose of uniform probe spacing. An Agilent 34401A multimeter was used as the voltmeter and a Keithley 6221 series current source was used to record I-V data manually. This set up was used to calculate the sheet and bulk resistivity of boron and phosphorus doped silicon samples.

2.9 Light-current-voltage (LIV) tester for IV curve

Photovoltaic cells are large PN junctions which generate electricity when the absorption of light provides energy to separate electron hole pairs within a cell. In the absence of light, a PV cell can be modelled as a current source in parallel with a diode. A voltage sweep of a diode with a source meter produces a current/voltage characteristic (IV) in which the current is exponentially related to an applied voltage [19].

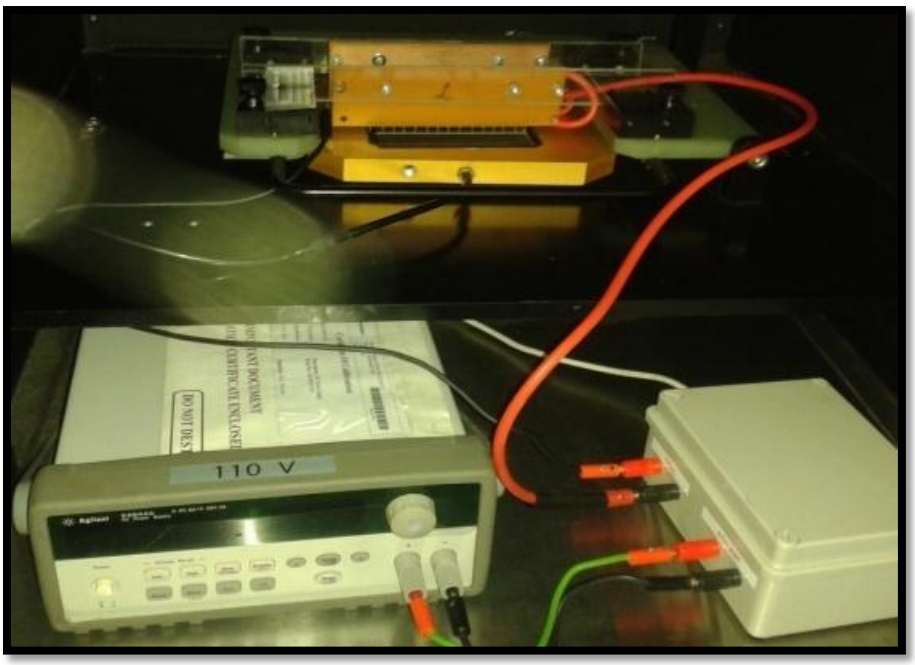


Figure 2.8 Front view of LIV efficiency measurement instrument

$$I = I_0\left(e^{\frac{qV}{nkT}} - 1\right) - - - - - - (2.7)$$

Here, I_0 is saturation current of the diode, q is the charge of an electron, V is the diode voltage, n is diode ideality factor, k is Boltzmann's constant, T is the Kelvin temperature.

When light is applied to the PV cell, the IV curve is a superposition of the IV in the dark (diode current) with the light-generated current I_L (photovoltaic current); light causes a shift of the IV curve down the y-axis into the fourth quadrant, and the equation becomes [19]

$$I = I_0\left(e^{\frac{qV}{nkT}} - 1\right) - I_L - - - - - - (2.8)$$

In this paper, Greetings incorporation LIV tester of one sun simulator for I-V measurement has been used. This instrument provides Aurum coated vacuum chunk as the bottom probe and tungsten probe at the top. The internal circuitry has the power supply with signal conditioning unit that follow the microcontroller unit that finally connected to the LAB VIEW interface. It has Xenon lamp light source that are optically filtered to match the AM 1.5G spectrum with spectral irradiance 1000W/m^2. Temperature is a major concern with this lamp-based solar simulator due to the generated heat reduces the open circuit voltage of the cell. So the samples are maintained at 25 °C ± 1 °C temperature.

2.10 Summary

The various techniques of semiconductor characterization is explained in this chapter. These techniques are having well established theory along with their implementation through instrumentation. Due to advance in computation techniques most of the data acquisition process was aided by appropriated software. During every measurement the instrument was calibrated using standard sample for validating the measurement. Calibration of the optical reflection measurement performed using a TRF 008 reference sample which reflects nearly 100% incident light. All optical measurement performed inside dark room to avoid any additional light source. SEM study allowed observing surface morphology. Calibration of four point probe instrument performed before each measurement using standard silicon sample. Study of electrical characterization the standard sample has been used to calibrate the illuminated I-V curve for the measurement process. Temperature dependant I-V data were taken so quickly so no temperature change occurs during the data acquisition.

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Chapter III

Characterization of Wafer

3.1 Introduction

In this chapter, a low cost indigenously made hot probe experimental setup and the experimental details is briefly described for wafer characterization. The chosen sample is p-type mono-crystalline silicon wafer. At first, it is necessary to measure the parameter of crystalline semiconductor such as type of the semiconductor by this setup. Besides the type, the voltage versus time curve for various temperatures gives the information of the semiconductor material behavior due to temperature variation. So that, it could help for the measurement of charge carrier concentration, impurity concentration and majority charge carrier concentration due to thermal effect. The hot probe characteristic graphs were plotted by origin pro8 graph plotter. This chapter also shows the measurement of other properties such as wafer thickness, resistivity etc.

3.2 Mono-crystalline silicon substrate

Mono-crystalline silicon wafer is used in the manufacturing of high performance solar cells. There are two ways of wafer manufacture process; one is czochralski (CZ) and another is float zone (FZ) process. Again there are two types of mono-crystalline wafer one is IC grade and another is solar grade silicon wafer. Since solar cells are less demanding than microelectronics that is why as structural imperfections are concerned. The use of silicon in semiconductor devices requires a much higher purity than metallurgical grade silicon. IC grade silicon has the purity of nine nines" (99.9999999%) whereas the solar grade silicon has the purity of six nines" (99.9999%) [1].

Currently available solar cells are made from bulk materials that are cut into wafers between 180 to 240 micrometers thick. These wafers are called commercial wafer. Single-crystal wafer are cut from cylindrical ingots that later cut as square shape called pseudosquare substrate [2]. Silicon has a crystalline structure, and it has grown under controlled conditions to exhibits certain desired and predictable

characteristics. As a starting material used for solar cell fabrication process called wafer or substrate so that it is necessary to characterize the substrate. Doped silicon becomes either p or n-type. Dopant atoms can either be "donors" or "acceptors." Donors increase the electron concentration in the silicon, whereas acceptors increase the hole concentration [3].

The aim is to fabricate the solar cell on commercial mono silicon wafer in order to reduce the wafer cost for this research. ReneSola Ltd. provides these wafers [4]. In parallel, IC grade single side polished mono silicon wafer have also used for few purposes. So that, wafer of different thicknesses has been used. The single side polished wafers are costly enough that's why before use they are cut by laser cutter into 2.2×2.2 cm^2 dimension. Malaysian based company Hamadatec Sdn. Bhd. provides the single side polished wafers [5]. Table 3.1 gives the information of the samples that has been used in this research.

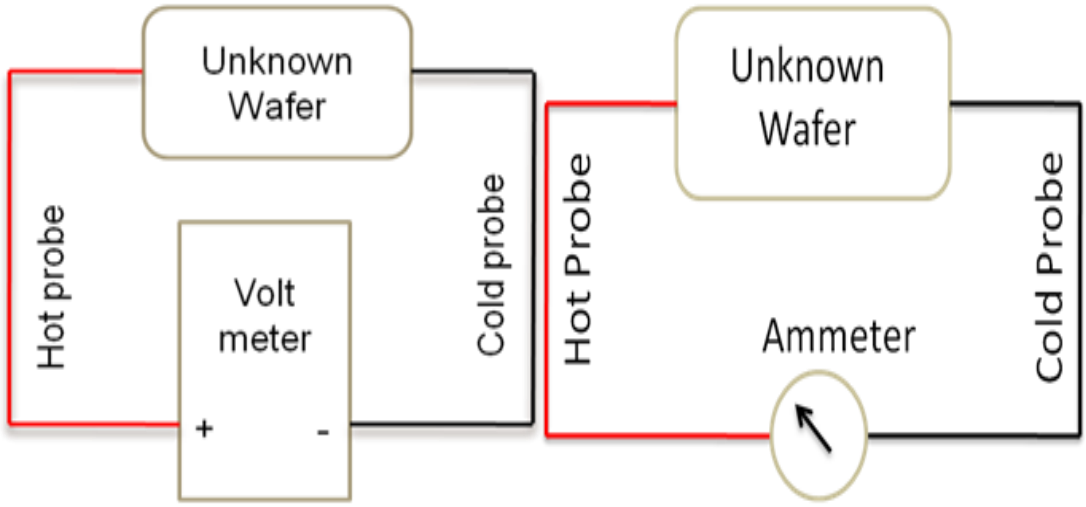
Table 3.1 Sample name, Thicknesses and the name of supplier

Sample no.	Sample name	Thickness (Company specification)	Name of supplier
Sample-1	p-type (100), Solar grade mono silicon wafer	180±20 µm	ReneSola Ltd., China
Sample-2	p-type (100), IC grade mono silicon wafer (single side polished)	600±50 µm	Hamadatec Sdn. Bhd., Malaysia

Before start with the fabrication process initially it is important to characterize the substrate. At first it is important to know the dopant type. Hot probe method is the simplest way to measure the wafer type. The next step is to measure the thicknesses of the wafer. A simple dial indicator has been used for this measurement. The measurement was accurate and easy. After that, the electrical properties such as sheet and physical resistivity were measured. For this purpose the four point probe method was used.

3.3 Hot probe theory

The simple "hot-probe" experiment by using a soldering iron and a standard voltmeter or center-zero milli-ammeter to distinguish between n-type and p-type semiconductors. By contacting a semiconductor wafer with a "hot" probe such as a heated soldering iron and "cold" probe at room temperature where hot probe is connected to the positive terminal of the meter and the cold probe is connected to the negative terminal and then measure the direction of current flow between the two probes. Positive voltage reading or ammeter deflection from left to right on the meter determines the material is n- type and the reverse is p-type. Current flows from the hot probe to the cold probe for the n-type wafer. Current flows in the opposite direction for the p-type wafer [6, 7]. Block diagram of a simple hot probe setup is shown in figure 3.1.



(a) (b)

Figure 3.1 Two alternate block diagram of hot probe measurement system

The explanation is that the thermally excited majority free charged carriers are diffused within the semiconductor from the hot probe to the cold probe. A temperature gradient generates potential differences called Seebeck voltage. For n-type semiconductor material, electron diffuses from hot to cold probe throughout the sample setting up an electric field that produces a potential difference, and then detected by voltmeter. Actually electron flows through the cold probe (negative terminal) and current (hole) flows in the opposite direction with the positive terminal hot probe, so that the voltmeter reading is positive. At the same time the ammeter deflects from left to right. Similarly for p-type, the situation is opposite, so that the

voltmeter reading is negative and the ammeter deflects from right to left [6, 7, 8]. If the current meter has zero resistance, and ignoring the (small) thermoelectric effect in the metal wires one can justify that the Fermi energy does not vary throughout the material. The corresponding energy band diagram illustrates the specific case in which the temperature variation causes a linear change of the conduction band energy as measured relative to the Fermi energy. As the effective density of states decreases with decreasing temperature, the conduction band energy decreases with decreasing temperature yielding an electric field which causes the electrons to flow from the high to low temperature. The same reasoning reveals that holes in a p-type semiconductor will also flow from the higher to the lower temperature [7].

3.4 Setup for measurement with hot probe

Figure 3.2 shows a low cost indigenously made hot probe that consists of a hot plate, a programmable temperature controller, a voltmeter, a temperature meter, contact probes and k-type thermocouple etc. which is not same as the conventional soldering iron hot probe system. Initially few portion of a semiconductor wafer was placed on hot plate and the rest part of the wafer was placed on cold nonconductive base. The in-house made hot probe was used to heat up the wafer up to 100˚C and two copper probes of this measuring tool measures potential difference between two probes, shown in figure 3.2. Predefined temperature was controlled by a low cost programmable temperature controller. Positive probe of the meter was connected to the hot plate side wafer and negative probe of the meter was connected to the cold plate side wafer. To measure the temperature of both hot and cold probe, two k-type thermocouples are connected in contact of the hot and cold surface of the wafer.

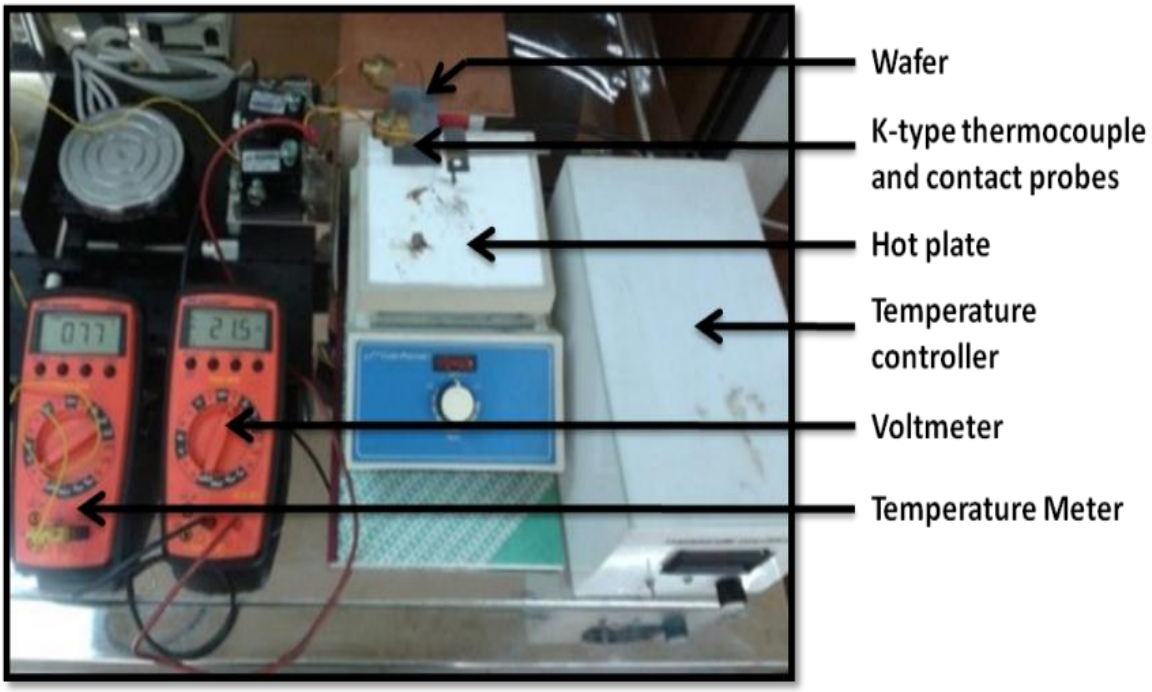


Figure 3.2 A low cost, in-house made hot probe setup

The conventional system was only used for measure the wafer type. But this in-house made hot probe system is used to measure the wafer type, thermal effect on majority charge carrier concentration and impurity concentration, doping uniformity etc.

3.5 Measurement for the type of material with hot probe

In this thesis the chosen mono-crystalline silicon substrate was p-type for solar cell fabrication. So initially it was needed to check that the selected wafer was either p-type or n-type.

In this procedure, the temperature was set first in the temperature controller then the 'Run' button was pressed and at the same time a regulatory knob of the hot plate was set low to high and then waited for few minutes to reach the predefined temperature. Portion of silicon wafer was placed on the hot plate where the rest was placed on a nonconductive base. Two k-type thermocouple placed simultaneously in contact with the hot and cold surface of the wafer to measure the temperature in situ for both hot and cold probes. The wafer began to heat up to 100˚C by the hot plate and thermally generated carriers started to diffuse through it from hot to cold portion. Two copper probes were connected with a voltmeter to measure the potential

differences (thermo-electrical voltage) between two probes. The red probe (positive) of the voltmeter attached on the hot side and black probe (negative) attached on the cold side of the wafer.

Table 3.2 Measurement of wafer type using indigenously made hot probe system

Sample no.	Name of sample	Voltage	Wafer type
Sample-1	p-type (100), Solar grade mono silicon wafer	-25 mV	p-type
Sample-2	p-type (100), IC grade mono silicon wafer (single side polished)	-0.9 V	p-type

The voltmeter shows negative readings that determines the material was p-type.

3.6 Wafer thickness measurement by dial indicator

The dial indicator of model no. 2110S-10, Mitutoyo, Japan was used for the measurement of wafer thicknesses. It has a single gauge at the centre and three legs to place the gauge on the wafer. In the gauge the spindle moves smoothly into the stem with less than 1.5 N pressures where it provides an involute curved lifting lever. In its dial there are two indicators. The smaller indicator indicates the number of complete rotation of the larger indicator.

Table 3.3 Measurement of wafer thickness using dial indicator

Sample no.	Thickness (company specification)	Measured thickness by dial indicator
Sample-1	180±20 µm	198 µm
Sample-2	600±50 µm	600 µm

3.7 Electrical properties measurement by four point probe

In this thesis, a four point probe set up by using a probe station of Cascade Microtech, D-01561 Sacka, Germany was used. The probe spacing was maintained 1

mm. An Agilent 34401A multimeter was used as the voltmeter and a Keithley 6221 series current source was used to record I-V data manually shown in section 2.8. This set up was used to calculate the sheet and physical resistivity of p-type wafer.

Sheet resistivity can be calculated from the Eq. 3.1 [9].

$$R_{sh} = 4.532\frac{V}{I} \text{.....(3.1)}$$

Physical resistivity can be calculated from the Eq. 3.2 [9]

$$\rho = 4.532\ t\ \frac{V}{I} \text{.....(3.2)}$$

Here, t is sample thickness.

Table 3.4 Resistivity measurement using four point probe techniques

Sample no.	Name of sample	Dimension of sample	Sheet resistivity using four probe	Thickness (Table 4.2)	Calculated Physical resistivity
Sample-1	p-type (100), Solar grade mono silicon wafer	125×125 mm^2	114.81 Ω/sq	198 µm	2.3 Ω-cm (Company specification: 1-3 Ω-cm)
Sample-2	p-type (100), IC grade mono silicon wafer (single side polished)	2.2×2.2 cm^2	145 Ω/sq	600 µm	8.7 Ω-cm (Company specification: 1-50 Ω-cm)
Sample-3	p-type (100), Solar grade mono silicon wafer	2.2×2.2 cm^2	141.41 Ω/sq	198 µm	2.8 Ω-cm (Company specification: 1-3 Ω-cm)

3.8 Hot probe characteristic curve analysis

In this thesis the hot probe characteristic curves measured in a bulk crystalline Silicon samples of two different thicknesses for the temperature range 50°C-80°C with an interval of 10°C. These curves demonstrates negative voltage measured between the two electrodes. The procedure has been explained in the section 3.5. By increasing the hot probe temperature, the measured voltage between electrodes is also increased. For various temperatures, the temperature gradient potential differences values had been recorded and plotted. Figure 3.3 shows the hot probe characteristic curves for two samples.

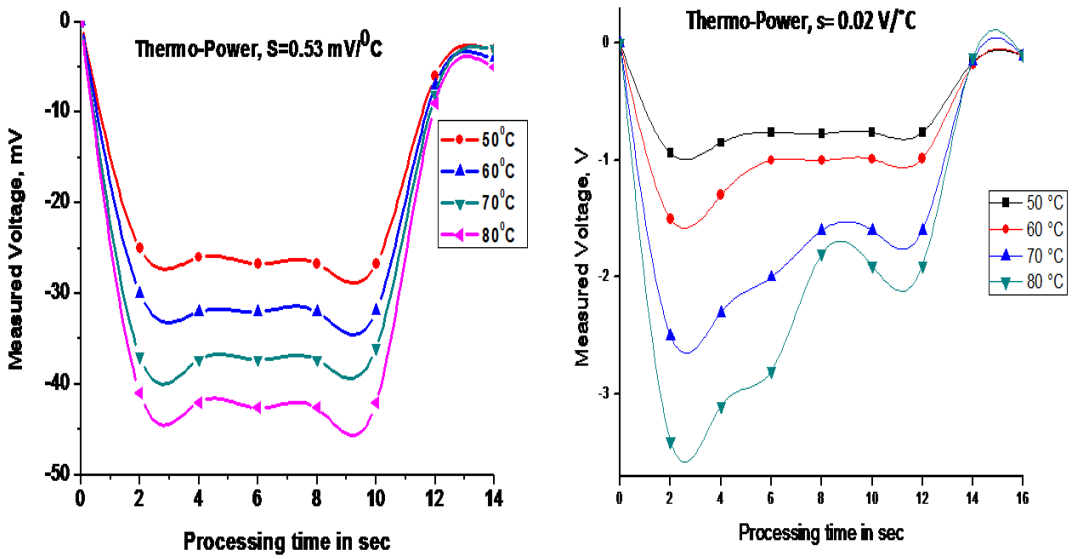


Figure 3.3 Hot probe characteristic curves for (a) sample-1 and (b) sample-2

The curves are almost similar to each other. Three different regions can be distinguished in the obtained characteristics those are described below

1. Heated carriers begin to leave the heated part of the wafer surface by a diffusion mechanism. As a result, a steep rise at the initial peak shows a built-in electric field which was developed between the electrodes.
2. Cold electrode would be simultaneously warmed up because of the diffusion of those heated carrier. So that, the built-in electric field tends to prevent the diffusion process and creates a steady state voltage. This steady state condition exists until the heated source was switched off.

3. When the hot plate was removed from the wafer then the thermally generated carriers return back to its initial states and this process is called recombination of the excited additional charged carrier generation [7].

Thermo-power can also be obtained by steady state voltage divided by temperature. The steady voltage obtained from the characteristic curves shown in the table 3.5. By using these data thermally excited charge carrier concentration, thermal effect on impurity concentration and majority charge carrier concentration can be calculated that is explained in section 3.9

Table 3.5 Thermo-power measurement using hot probe characteristic curve

Temperature (˚C)	Sample-1		Sample-2	
	Steady state voltage	Thermo-power	Steady state voltage	Thermo-power
50˚C	-26.7 mV	0.053 mV/˚C	-0.76 V	0.02 V/˚C
60˚C	-32 mV		-0.99 V	
70˚C	-37.3 mV		-1.6 V	
80˚C	-42.64 mV		-1.9 V	

3.9 Thermal effect on carrier concentration

In this section, the effect of temperature on impurity concentration and majority charge carrier concentration have been measured by hot probe measurement set up for the p- type mono silicon sample. Theoretical results taken by solving basic conductivity equation of semiconductor and it gave the thermally generated carrier Δp values. The chosen temperature range was 50°C-80°C with an interval of 10°C. By solving Continuity and Poisson's equation [7, 8] with error function and from the hot probe characteristic curves, thermally generated carrier Q values were obtained. The experimental and theoretical results are compared between Δp and Q values.

3.9.1 Equation for thermally excited charge carrier concentration and impurity concentration

Thermally excited charge carrier concentration can be found by solving the conductivity behavior equation in semiconductor and Boltzmann relation. Note that, for p-type semiconductor neglecting donor ion concentration N_D and p is the majority charge carrier. But at higher temperatures, this p values differ from the intrinsic carrier concentration at T temperature (n_{iT}). Assume that, for the temperature variation from room temperature to 150°C, the effective masses of the charge carriers and semiconductor bandgaps are stable [7, 8, 10].

$$\Delta p \approx \frac{{n_i}^2 R^2}{N_A} \quad \text{.....(3.3) [7, 8]}$$

Where,

$$R = \frac{n_{iT}}{n_i} = \left(\frac{T}{T_0}\right)^{3/2} e^{\frac{E_g}{2KT_0}\left(1-\frac{T_0}{T}\right)} \quad \text{.....(3.4)}$$

Where, R is the function of heating temperature

n_i is the intrinsic carrier concentration

n_{iT} is the carrier concentration at T temperature

T is the increased temperature

T_0 is the room temperature

N_A is the acceptor concentration

Δp is the thermally excited charge carrier concentration

At room temperature, the acceptor concentration (N_A) has been calculated from

$$\rho = \frac{1}{q\mu_p N_A} \quad \text{.....(3.5) [11]}$$

Where, (μ_p) is the hole mobility

ρ is the physical resistivity of the wafer.

Variation of hole mobility with respect to temperature is shown in figure 3.4 [12].

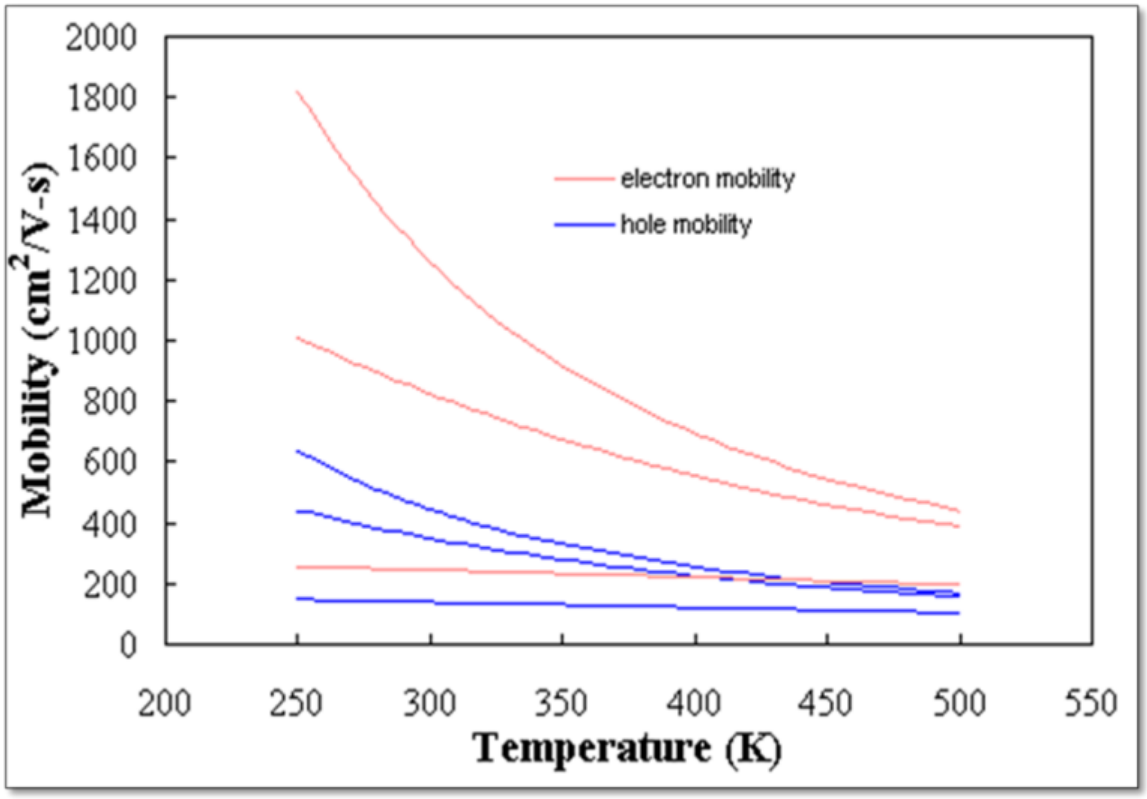


Figure 3.4 Carrier mobility versus temperature for silicon [12]

3.9.2 Results

The acceptor concentration at room temperature can be calculated from equation (3.5) where hole mobility (μ_p) is $\sim 450 cm^2/V \cdot s$. The result is shown in the table 3.6.

Table 3.6 Acceptor concentration at room temperature with respect to physical resistivity

Sample no.	Sample name	Thickness (See Table 3.3)	Physical resistivity (See Table 3.4)	Acceptor Concentration at room temperature
Sample-1	p-type (100), Solar grade mono silicon wafer	198 µm	2.3 Ω-cm	6×10^{15} atom/cm^3
Sample-2	p-type (100), IC grade mono silicon wafer (single side polished)	600 µm	8.7 Ω-cm	1.59×10^{15} atom/cm^3

The characteristic curves for p-type silicon wafers were taken at the temperature range 50°C-80°C with an interval of 10°C is shown before in figure 3.3. The hole mobility decreases with temperature increases that is shown in figure 3.4. The calculated value of impurity concentration (N_A), function of heating temperature (R) and thermally excited charge carrier density (Δp) from equation (3.5), (3.4), (3.3) are shown in the table 3.7.

Table 3.7 Temperature dependent hole mobility (μ_p), impurity concentration (N_A), function of heating temperature (R) and thermally excited charge carrier density (Δp)

Temperature T (˚C)	μ_p ($cm^2/V \cdot s$)	R	Sample-1		Sample-2	
			N_A ($atom/cm^3$)	Δp ($atom/cm^3$)	N_A ($atom/cm^3$)	Δp ($atom/cm^3$)
50	≈ 400	5.52	6.79×10^{15}	0.45×10^{6}	1.79×10^{15}	0.17×10^{7}
60	≈ 370	10.66	7.344×10^{15}	0.15×10^{7}	1.9×10^{15}	0.59×10^{7}
70	≈ 345	20.26	7.87×10^{15}	0.52×10^{7}	2.07×10^{15}	0.19×10^{8}
80	≈ 325	36.74	8.36×10^{15}	1.6×10^{7}	2.21×10^{15}	0.61×10^{8}

These theoretical findings of thermally excited charge carrier density (Δp) are then compared with the values of experimental results shown in section 3.9.4.

3.9.3 Thermally excited charge carrier concentration by using Poisson's equation

Thermally excited charge carriers leave the heated zone of the wafer and create a depletion region around the hot probe. These thermally excited charge carrier concentration (Q) can be found by solving the Poisson's equation and Gauss distribution written in equation (3.6)[7, 8].

$$Q = \frac{-V 2\pi^{\frac{3}{2}} \varepsilon_0 \varepsilon_r 4Dt}{qL^2} \quad \text{.....(3.6)}$$

Where, negative sign indicates that the material is p-type [7, 8].

D is the diffusion coefficient of the charge carriers.

V is the steady state voltage

t is the time interval between the initial state and steady state

L is the probe distance

ε_0 is the absolute permittivity

ε_r is the relative permittivity

The diffusion coefficient for p-type semiconductor (D_p) described by well-known Einstein equation [13]

$$\frac{D_p}{\mu_p} = \frac{KT}{q} \quad \text{.....(3.7)}$$

Where, μ_p is the hole mobility.

3.9.4 Experimental Results

According to Eq. (3.6), quantity of thermally excited charge carrier could be analyzed.

The steady state voltage from table 3.5 has been used in this section. Time interval between the initial state and steady state was approximately t=5 seconds which is shown in figure 3.3. Here probe distance was maintained at L = 5cm.

For the calculation, few additional data for silicon sample has been used such as absolute permittivity, $\varepsilon_0 = 8.854 \times 10^{-14}\ F/cm$, relative permittivity, $\varepsilon_r = 11.64$ and charge quanta, $q = 1.6 \times 10^{-19}$C . The experimental values of thermally excited charge carrier density (Q) are shown in table 3.8. Table 3.8 also shows the values of temperature dependent steady state voltage and hole diffusion coefficient (D_p). Finally, comparison between theoretical and experimental values is shown in table 3.9.

Table 3.8 Temperature dependent steady state voltage, hole diffusion coefficient (D_p) and thermally excited charge carrier (Q)

Temperature (T˚ C)	Hole diffusion coefficient (D_p)	Sample-1		Sample-2	
		Steady state voltage (mV) [table 3.4]	Thermally excited carrier (Q) (atom/cm^3)	Steady state voltage (V) [table 3.4]	Thermally excited carrier (Q) (atom/cm^3)
50	11.08	-26.7	1.7×10^7	-0.76	4.8×10^8
60	10.6	-32	1.9×10^7	-0.99	5.9×10^8
70	10.17	-37.3	2.2×10^7	-1.6	9.2×10^8
80	9.87	-42.64	2.4×10^7	-1.9	10.7×10^8

Table 3.9 Comparison between theoretical and experimental values of thermally excited charge carrier concentration

Temperature (T°C)	Sample-1		Sample-2	
	Δp (atom/cm^3)	Q (atom/cm^3)	Δp (atom/cm^3)	Q (atom/cm^3)
50	0.45×10^6	1.7×10^7	0.17×10^7	4.8×10^8
60	0.15×10^7	1.9×10^7	0.59×10^7	5.9×10^8
70	0.52×10^7	2.2×10^7	0.19×10^8	9.2×10^8
80	1.6×10^7	2.4×10^7	0.61×10^8	10.7×10^8

Finally, the majority charge carrier hole can changes due to thermal effect that can explain by the following equation.

$$p_T - p = \Delta p \quad \text{.....(3.8)}$$

Where, p is the majority charge carrier

p_T is the majority charge carrier changes to p_T due to thermal effect

∇p is the thermally excited charge carrier density

3.10 Summary

An approach of using a low cost in-house made hot probe is used to determine the wafer types for mono-crystalline silicon sample. Wafer thickness was measured by dial indicator. Sheet resistivity and physical resistivity was measured by four point probe. The steady state voltage values were found from hot probe characteristic curves for temperature 50˚C -80˚C. The majority charge carrier and impurity concentration can be changed by thermal effect. These can be measured by hot probe set up. The theoretical results found from solving basic conductivity equation of semiconductor. The experimental values put on the equation that solved from Continuity and Poisson's equation with error function. The theoretical and experimental values of thermally excited charge carrier are finally compared. Table 3.8 shows the values between the ranges 10^7 to 10^8 for sample-1 and sample-2.

The critical part of this experiment was to measure the surface temperature of silicon wafer as many circumstances can contribute to faulty temperature reading. Good contact was made for the sample and the hot plate as well as from silicon wafer to thermocouple. Possible heat loss in the system might not be an issue here as the hot probe and the thermocouple have been kept in close vicinity: also kept the contact area for both the contacts as small as possible. In future a significant enhancement could be made to this same experiment by conducting the experiment in vacuum to avoid this kind of estimation. Another point is thermally conducting paste could be used between those contacts to improve the thermal conduction. The measurement of thermo-generated voltage between hot and cold probe and estimation of majority charge carrier concentration agrees with value from conventional measurement. Thus the low cost indigenously made hot probe, the theoretical estimation and the results of the study are expected to serve as a useful reference for the related research endeavor.

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Chapter IV

Properties of Chemically Etched Silicon Wafers

4.1 Introduction

This chapter described briefly the sample cleaning and texturing procedures. Standard RCA process has been used for sample cleaning and texturing [1, 2]. For that purpose, NaOH and De-ionized (DI) water has been used for sample cleaning and KOH, IPA and De-ionized (DI) water for texturing. The cleaned and textured samples were prepared for optical and structural characterizations. The optical characterization had done by spectroscopic reflectometry measurement. Structural characterizations had taken for textured sample by using stylus surface profilometer. Topographical images were found from scanning electron microscopy. The instrumental details of the spectroscopic reflectometer, stylus surface profilometer and scanning electron microscopy are discussed in chapter II.

4.2 Necessity for isotropic and anisotropic etching

One of the first steps in solar cell processing is the saw damage removal and texturing of mono-crystalline wafers. The Czochralski silicon (solar grade) wafers have micrometer sized surface damages. This layer caused by mechanical saw damage on the surface when it is cut from the ingot. This layer may contain abraded metal due to sawing and grinding abrasive due to polishing. This surface saw damage needs to be etched off (isotropic etching) at the beginning of the solar cell fabrication by several microns on both sides.

In order to remove the organic and inorganic contaminants from sample surface there are several procedures. Some procedures such as standard piranha solution (H_2SO_4:H_2O_2=3:1), standard NaOH or KOH with >5% solution (NaOH:H_2O=1:10), standard HNO_3 and HF solution (HNO_3:HF=50:1) can remove the saw damage contaminants [1, 2, 3]. NaOH aqueous alkali solution to remove the

saw damage layer has been used. Before use this solution it is need to know details either it is hazardous to health or environment. According to hazard statement (CLP regulation), >5% solution causes severe skin burns and eye irritation causing health damage. It is non flammable chemical and corrosive. For protection, Good ventilation is necessary. During cleaning gloves, safety eye glasses and appropriate vinyle (PVC) gloves have been used. The chemical etching procedures were carried under fume hood [4].

In order to increase the light trapping by multiple reflections it is important to produce homogeneous surfaces which are fully covered with four sided random pyramids of small sizes. Few parameters are important for this pyramidal growth process such as chemical concentration, etching time, temperature etc. Some procedures such as standard KOH/IPA solutions, Na_2CO_3/$NaHCO_3$ solutions, NaOH/carbohydrate solutions can causes anisotropic texturing. Standard KOH alkaline solution and IPA (iso2 propanol/ isopropyl alcohol) the etchant solution for anisotropic texturing had been used during solar cell fabrication [1, 3, 5]. Before use this solution it needs to know details either it is hazardous to health or environment. According to hazardous substance fact sheet isopropyl alcohol (IPA) is a colorless liquid. Inhaling isopropyl alcohol can irritate the nose and throat causing coughing and wheezing. It can irritate and burn the skin and eyes when contact. It is a flammable liquid and dangerous fire hazard. KOH is highly corrosive and it can severely irritate and burn the skin and eyes leading to eye damage. Its contact can irritate nose, throat and lungs. It is not flammable. For protection, Good ventilation is necessary. During cleaning gloves, safety eye glasses and appropriate vinyle (PVC) gloves have been used. The anisotropic chemical etching procedures were carried under fume hood [6, 7].

After each etching procedures had done the wafer has been rinsed into 2% HF solution. The aqueous solution of HF is clear, colorless, and highly corrosive liquids. When exposed to air it produces pungent fumes, which are also dangerous. It causes immediate and severe burning pain due to destruction of deep tissue layers. HF contact with the eye can cause eye burns and destruction of the cornea. For these reason proper precautions is necessary to handle HF solutions. For proper protection, protective clothing such as laboratory coat and acid resistant apron, shoes and long

pants must need. In addition, full face shield in conjunction with goggles, gloves etc. have been used [8].

4.3 RCA cleaning and texturing process

This thesis deal with p-type, (100) oriented, mono crystalline silicon wafer. The wafers generally contain micrometer size surface damages due to sawing and grinding. Solar grade silicon wafer contain more surface damages than IC grade one side polished wafer. In order to remove those surface damages it has been used standard RCA cleaning by concentrated solution of NaOH in de-ionized water (DI-W). The dissolving of caustic soda in water may be accompanied by heat release [4].

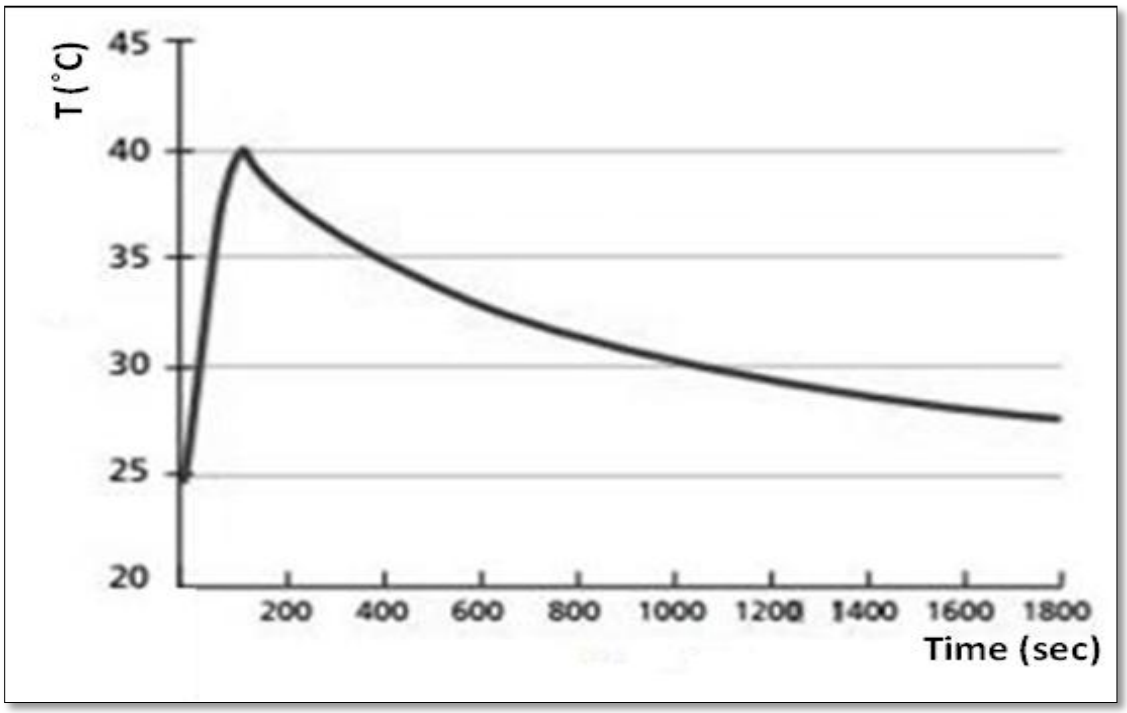


Figure 4.1 Dissolved NaOH in water, release heat [4]

10% NaOH solution, at 70°C temperature for about 10 minutes of isotropic etching removes the surface damages. Initially the DI water was put into the beaker and placed the beaker on the hot plate or the heater. When the temperature was raised to 30˚C the NaOH pellets were put into the beaker and waited until the temperature had risen to 70˚C. Then the wafers were put into the beaker for 10 minutes. After that wafers were rinsed into HF (2%) for 10 seconds into DI water for 1 minute and then dry with nitrogen blow.

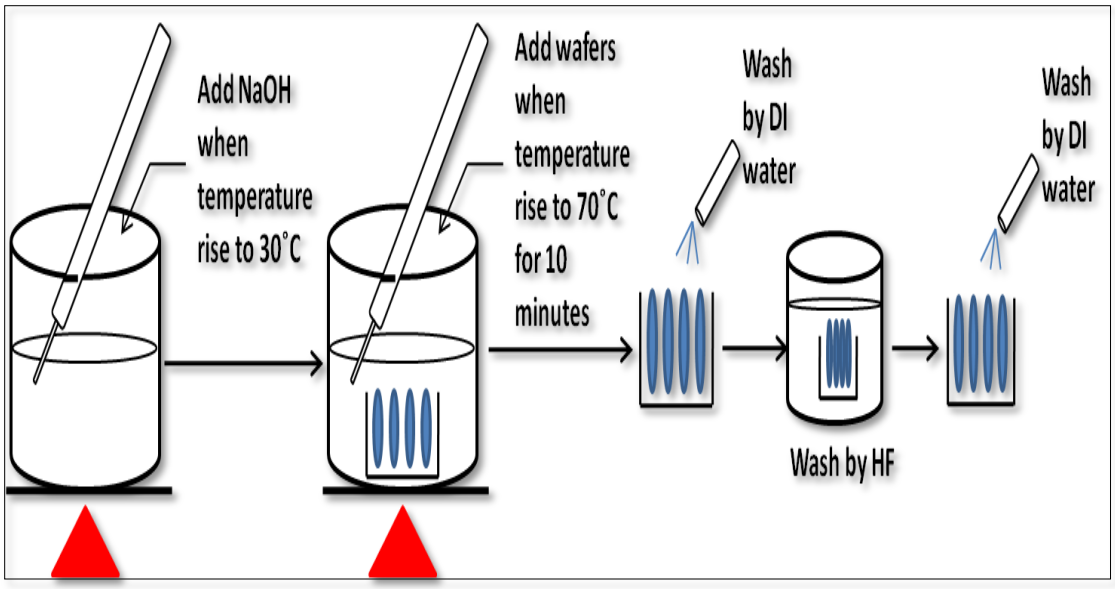


Figure 4.2 RCA cleaning for silicon sample preparation

In order to reduce the reflectivity of the wafer surface and to trap the light in the solar cell the texturing technique had been developed. Surface texturing depends on rate of reaction at the silicon sample surface and reactants rate that diffuse into the surface. These two processes control the rate of micro structural pyramid growth on the sample surface [2]. KOH, IPA (Iso2 propanol) and DI water have been used for the texturing process. IPA acts as an initiator of pyramid growth process by leading to a micro-masking of the surface [5]. High concentrations of KOH and low concentrations of IPA lead to a small number of pyramid starting points and high etch rate. Therefore pyramids become very large and there are still blank areas on the surface. The aim is to grow the pyramids on the entire sample without blank space. So the wafer has been textured in a solution consisting of comparatively low percentage of KOH and a high percentage of IPA [5]. A standard RCA texturing process has been followed where KOH, IPA (Iso2 propanol) and DI water with a ratio1:5:125 at 70°C temperature for about 10 minutes could grow pyramidal surface texture. After that wafers were rinsed into HF (2%) for 10 seconds, DI water for 1 minute and then dry with nitrogen blow.

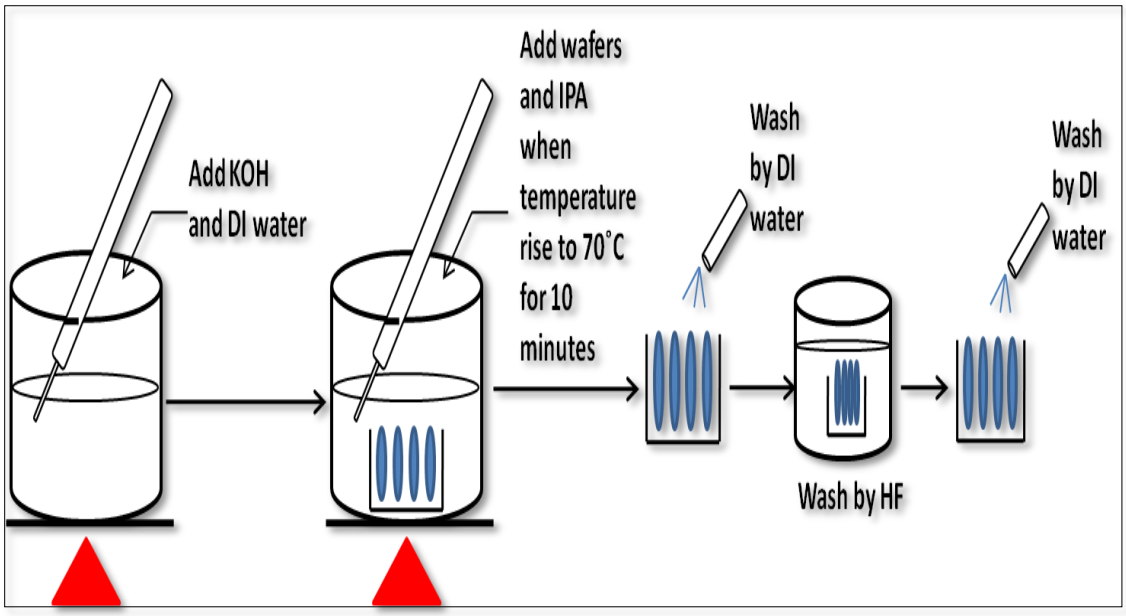


Figure 4.3 Texturing procedures for silicon sample

4.4 Thickness of textured silicon sample

At the beginning of the process it needs to be etched off the electrically inactive or dead layer or surface saw damage from the wafer surface. The process is isotropic etching that can etch several microns on both side of the wafer. The etching rate of silicon depends on product of hydroxide ions and free water concentration. Note that recently ingot cutting technology has been significantly improved. The anisotropic texturing also etched off both side of the sample due to pyramid formation. But the anisotropic etching rate is much less than isotropic etching. Note that the mirror polished wafer is not suitable for higher wetability and therefore leads to non uniform nucleation of pyramid. After both etching procedure we need to measure the thickness of the silicon wafer. Dial indicator of model no 2110S-10, Mitutoyo, Japan was used for the measurement of wafer thicknesses [section 2.2].

4.4.1 Results

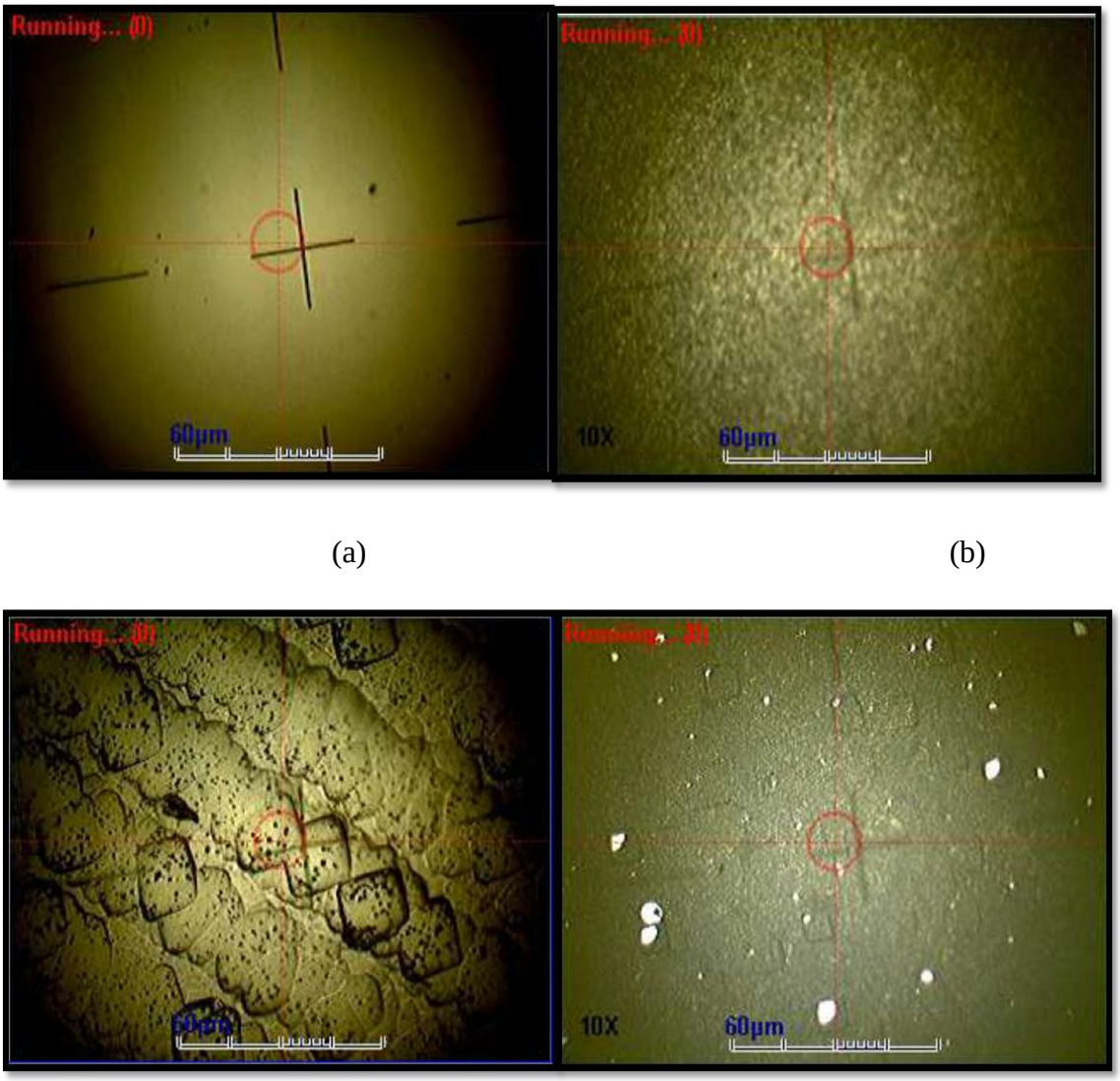
Table 4.1: Thickness comparison table for raw and textured mono silicon sample

Sample no.	Name of sample	Measured thickness	
		Raw sample	Textured sample
Sample-1	p-type (100), Solar grade mono silicon wafer	198 µm	194.8 µm
Sample-2	p-type (100), IC grade mono silicon wafer (single side polished)	600 µm	597.8 µm

4.5 Structural characterization

4.5.1 2D optical imaging

Optical microscope developed by Radiation Technology Company Ltd. (Taiwan) for optical imaging was used as a primary tool for viewing surface morphology of raw, cleaned, textured and diffused silicon wafer. 2D images of silicon surface was taken using bright field microscopy where light falls vertically on the top surface of the sample. Bright field microscopy is useful to observe the sample surface topography. Figure 6.4 shows the camera image from the reflectometer.



(a) (b)

(c) (d)

Figure 4.4 2D optical images with magnification 10X for sample-1 (a) SiCr reference sample for calibration (b) raw silicon wafer (c) cleaned silicon wafer (d) textured silicon wafer

4.5.2 Scanning electron microscope imaging

SEM was used to characterize the surface topography. In the case of raw silicon sample the substrate has prepared from sawing that shows the surface roughness which is shown in figure 4.5 (a). After saw damage removal process or isotropic etching the wafer becomes polished. The isotropic etching reduces the surface roughness and gives the wafer shiny look. The SEM image represents the shiny look is shown in figure 4.5 (b). The anisotropic etching produces the surface

roughness by growing micron sized pyramids which covers the whole surface. The top points of four sided pyramids are much brighter than the base portion because of the light reflection. Figure 4.5 (c) and (d) shows the pyramidal textured surface for sample-1 and sample-2.

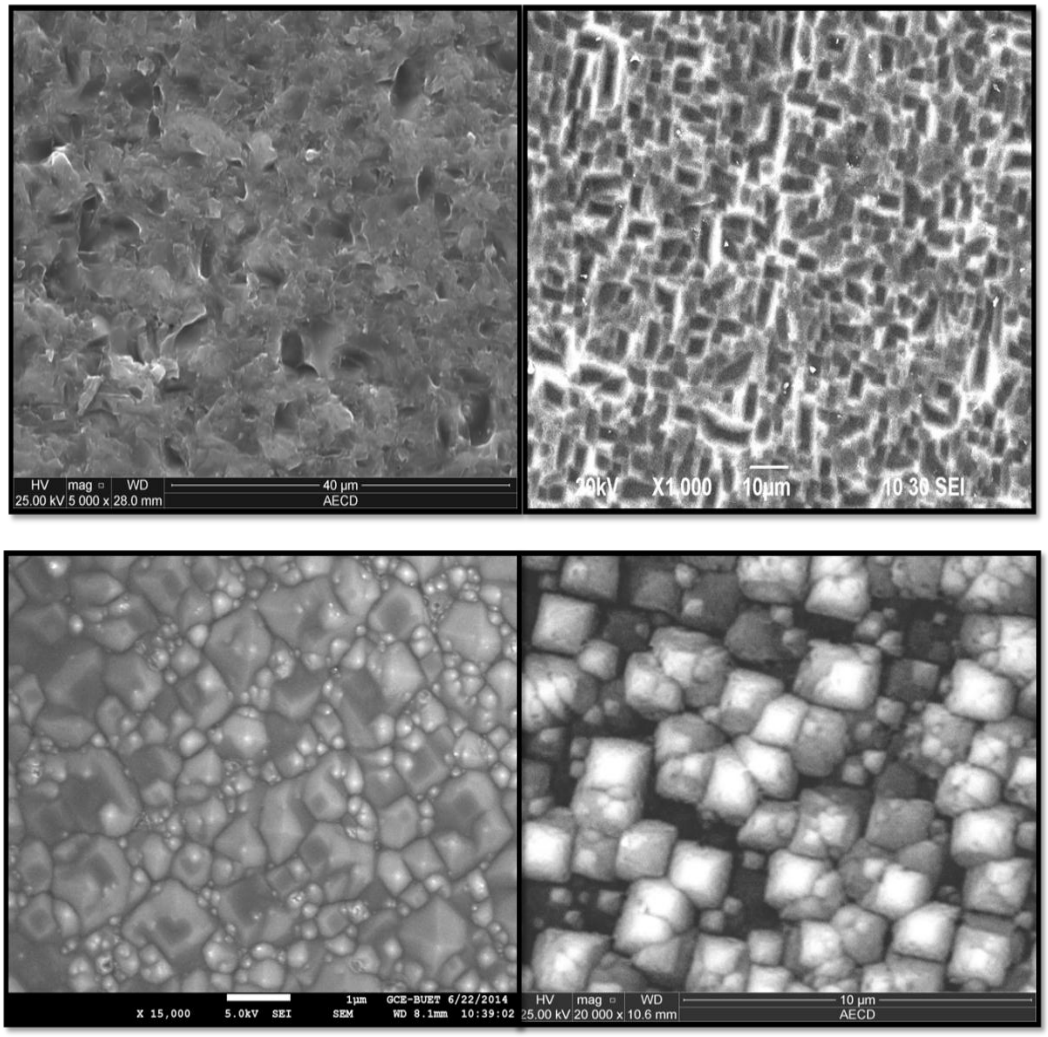


Figure 4.5 SEM images of silicon sample-1 (a) Raw wafer (b) Saw damage removed wafer

(c) textured silicon wafer (d) textured wafer of silicon sample-2

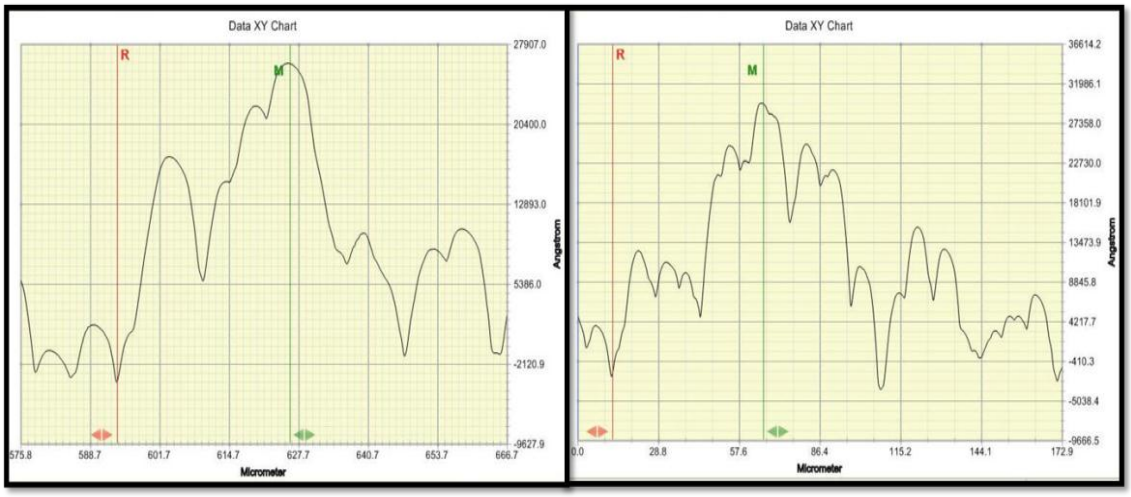
4.5.3 Pyramid height measurement by stylus surface profilometer

A high sensitive stylus profilometer, Dektak 150 from Veeco was used in this measurement. The stylus has diamond tip that is moved front to back of the surface (single scan direction) in contact and measures deflections of the stylus tip. It can be used to measure step heights (film thickness), surface roughness, waviness and stress. The stylus radius is 12.5µm and the stylus force during measurement is 3 mg. There

are reference (R) cursor and measurement (M) cursor that define the portion of the profile trace for leveling or performing analytical functions. One can adjust the bandwidth at each cursor to average the data points within the cursor's bandwidth. This is useful for leveling and average step height measurements. Average Step Height (ASH) Measures the difference between the average heights of the values in the M-cursor band minus the average height values in the R-cursor band. Vertical distance is close to ASH. The vertical distance measures the difference between the heights of the M-cursor minus the height of the R-cursor. This does not include average values of the cursor bands. Measurements are calculated as if the cursor bands have zero width. Before handle this instrument it is important to know that high voltage supplied to certain areas of the system is dangerous and can cause injury. The step heights higher than 1mm will break the stylus [9, 10].

4. 5.3.1 Results

As the textured wafer surface provides four sided pyramids, an approach has been taken to measure the roughness of the sample. For this measurement the first thing is to get step height between M cursor and R cursor. This step height can describe further as the four sided pyramid height. The measurement technique was very simple and easy. Figure 4.6 shows the surface roughness profile for sample-1.



(a) (b)

Figure 4.6 Sample 1 (a) and (b) Surface roughness profile

The pyramid height for sample-1 was found from the stylus surface profiler graph from figure 4.6 shown in table 4.2.

Table 4.2 Measurement of pyramid height using stylus surface profilometer

No. of measurement	Sample no.	Average Step height (µm)	Vertical Distance (µm)	Pyramid Height (µm)
1	Sample-1	2.9730 µm	2.9733 µm	~□2.97 µm
2		3.1198 µm	3.1212 µm	~□ 3.12 µm

4.6 Optical Characterization

4.6.1 Light reflectivity measurement by Spectroscopic Reflectometer

Spectroscopic reflectometer uses optical technique to measure the thickness of thin transparent and semi-transparent films by analyzing white light interference. The incident light falls normal to the sample surface so it is less expensive and much simpler than ellipsometry. In this research work this spectroscopy has used for the percentage of light reflection observation from the silicon sample that is why we can compare among raw, cleaned, textured and even doped sample. In this purpose we have used SR from Radiation Technology Company Ltd. (Taiwan). Figure 4.7 shows the functional unit of the reflectometer [11].

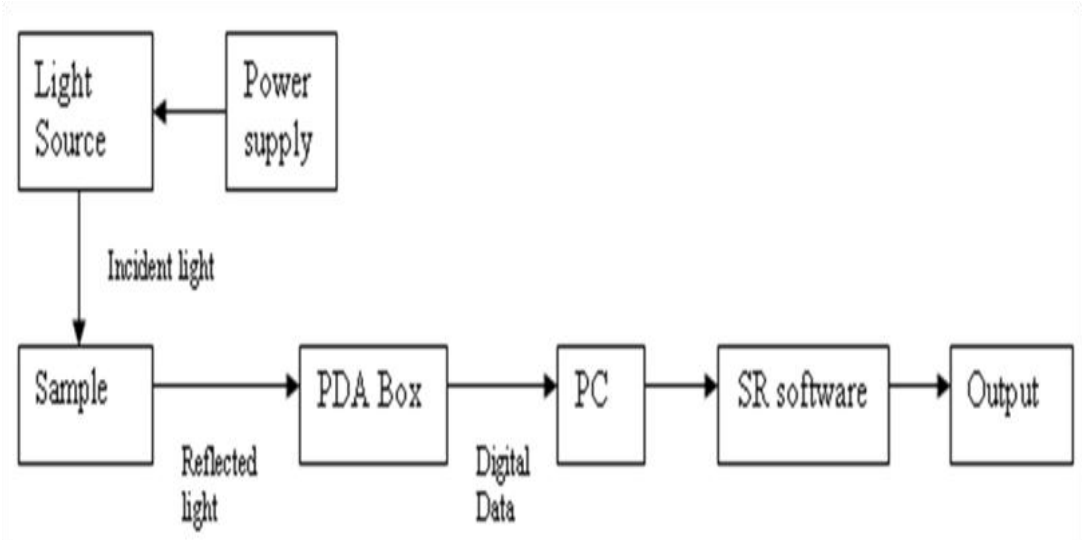
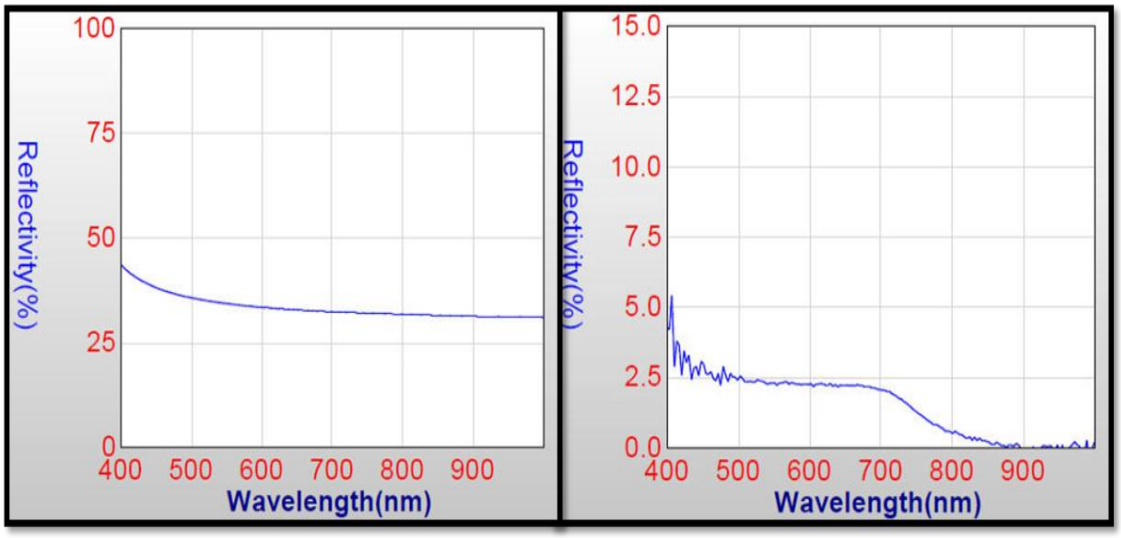


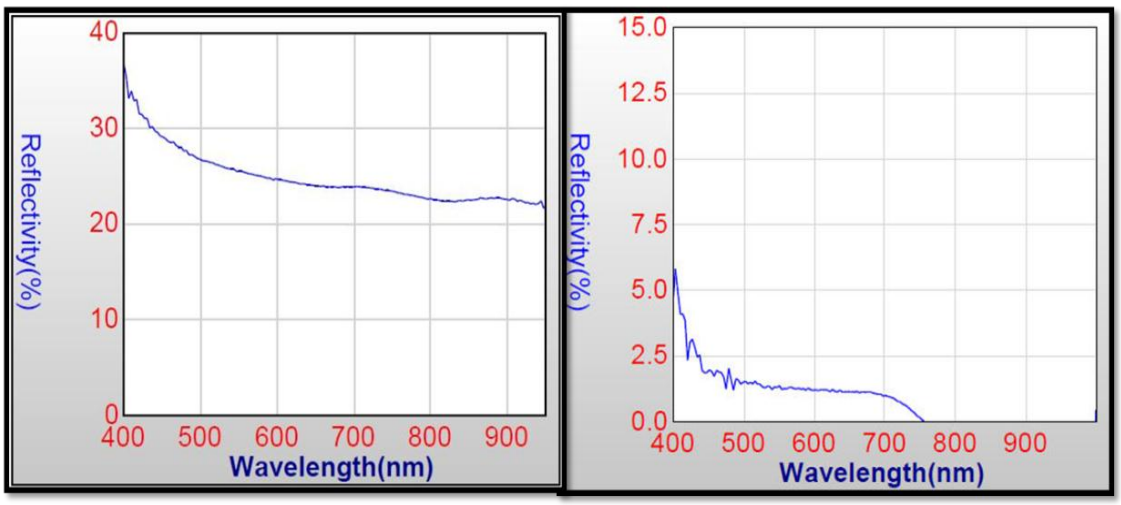
Figure 4.7 Block diagram of spectroscopic reflectometer [11]

4.6.1.1 Results

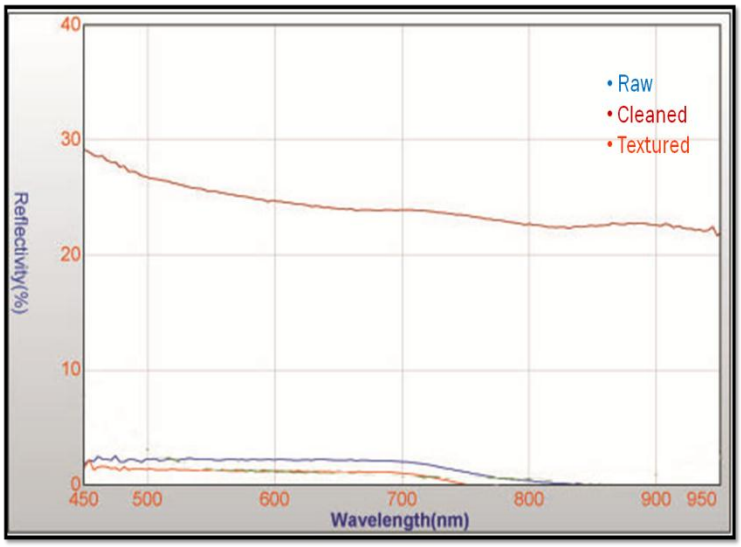
The SR software gives the wavelength versus percentage of reflectivity (average reflectance factor) graph. Note that its spectral range is 380 nm -1000 nm. Wavelength versus %reflectivity graph is shown in figure 4.8. Figure 4.8 (c) shows the %reflectivity much higher value for the cleaned or saw damage removed sample. Note that, in this measurement low cost solar grade mono silicon wafer of about 200 micron (commercial silicon wafer) wafer has been used. This wafer has two sided rough surfaces. Isotropic cleaning procedure not only removes the organic contaminants but also reduces the surface roughness. That is why the average reflectance factor increases in the cleaned wafer.



(a) (b)



(c) (d)



(e)

Figure 4.8 (a) Reflectivity graph of SiCr reference sample for calibration. %Reflectivity versus wavelength graph for silicon sample-1(650-800 nm) (b) %Reflectivity for raw silicon wafer is about 2.4% (c) %Reflectivity for cleaned silicon wafer is about 24% (d) %Reflectivity for textured silicon wafer is about 1% that is reduce by multiple reflection from the pyramid growth (e) Comparison of %reflectivity for raw, cleaned and textured silicon wafer.

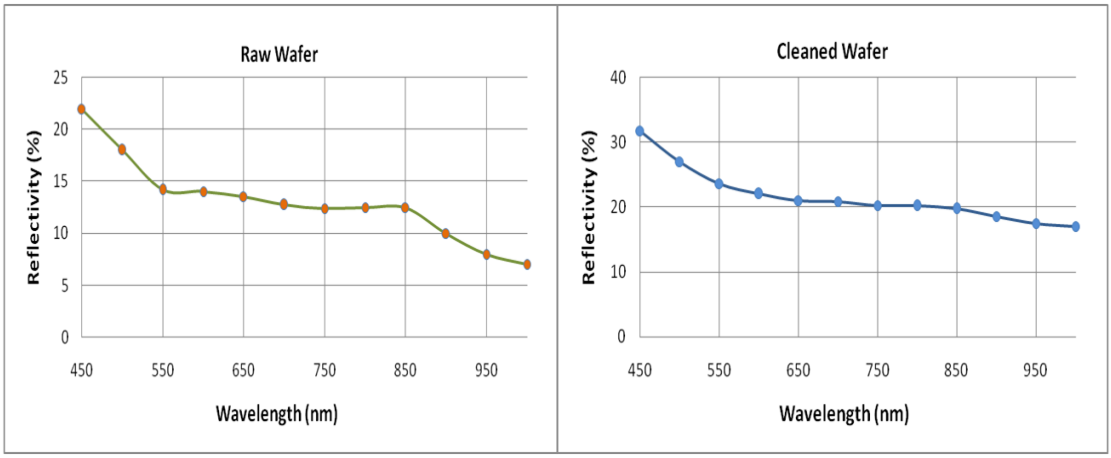
4.6.2 Light reflectivity measurement by Spectral Reflectance Measurement

The light reflectance was also measured by spectral reflectance measurement (SRM) system. It is a simple, low cost, computer-controlled, normal light incidence measurement system. It is consist of a stepper motor driven mini monochromator where the spectral range is 400-1200nm. Unlike the spectroscopic reflectometer, the incident light is not focused in a point. So a spread incident light of almost one inch diameter was incident on the sample. Light comes from the exit slit of the monochromator that is guided to the wafer at near normal incidence. Stepper motor is used to vary monochromator output wavelength. A light chopper is placed at the exit slit of the monochromator to provide reference signal to the lock-in to ensure all the stray light is rejected by the system and enhance system sensitivity from nano volt to mV range. Surface reflection as a function of wavelength is determined by measuring photodetector response. In order to determine spectral response, the sample at first

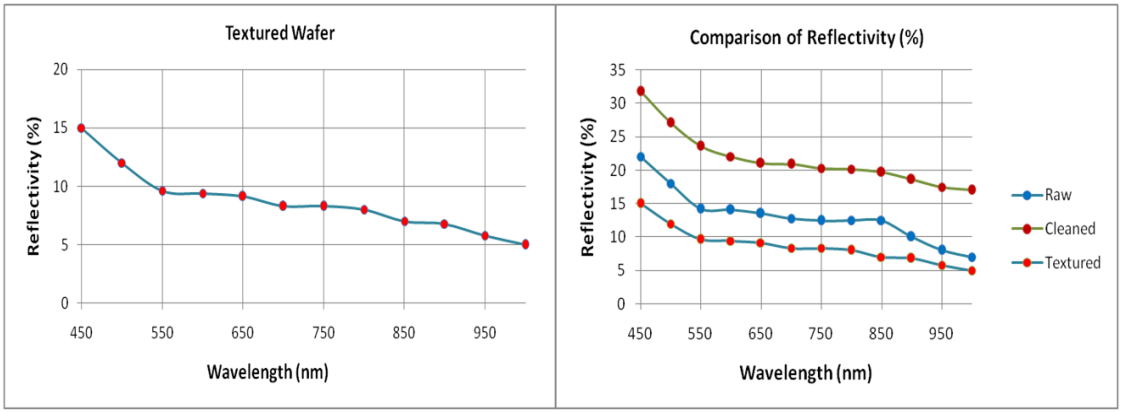
placed on vacuum chunk with top and bottom contact for probing. A LabVIEW interface is used for data acquisition [section 2.3.2].

4.6.2.1 Results

At first the data was taken from the mirror reflection instead of the sample. Then the data of raw, cleaned and textured silicon wafer was taken. All the graphs gave us light reflection versus wavelength data. Light reflection were in arbitrary unit (AU). So it needs to convert those data into percentage of reflectivity(%) [Appendix II]. For this process, divide the sample data by mirror data and multiply it by 100 to get the %reflectivity. These are done by Microsoft Office Excel 07. Figure 4.9 shows the SRM graph of %reflectivity versus wavelength (nm). Compare these results with the results of Spectroscopic Reflectometer one can find the graph pattern are same except the values. The main reason for this, the incident light width on the sample was not same. In the SRM measurement the diameter of the incident light was almost one inch. In the Spectroscopic reflectometer, the diameter of the incident light was less than 0.5 mm.



(a) **(b)**



(c) **(d)**

Figure 4.9 %Reflectivity versus wavelength graph for silicon sample-1 (650-800nm) (a) %Reflectivity for raw silicon wafer is about 13% (b) %Reflectivity for cleaned silicon wafer is about 21% (c) %Reflectivity for textured silicon wafer is about 8% that was reduced by multiple reflection from the pyramid growth (d) Comparison of %reflectivity for raw, cleaned and textured silicon wafers.

4.7 Summary

In this chapter the RCA cleaning and texturing details for mono silicon sample is explained. The cleaning and texturing process is also called isotropic and anisotropic etching where alkali solution was used. Texturing process needs iso2-propanol (IPA) for pyramid growth. The appropriate precaution should be maintained before the use of IPA and HF solution is also described. As the cleaning and texturing procedures are the part of fabrication, it is essential to characterize the samples after each stage of fabrication. Characterization helps to check the fabrication process is ok. For this purpose the wafer thickness was measured. The isotropic and anisotropic etching causes the loss of thicknesses, where isotropic etching is more responsible than anisotropic etching. 2D Optical microscope images were shown in this chapter. The images were taken by SR tool with 10X magnification. The surface topography was analyzed by SEM. It shows the clear topographical images of the silicon wafer in every step. It shows the difference among the fabrication steps. Initially the surface was rough due to sawing. In the textured sample surface it is also rough but the roughness was formed by repetitive growth of the four sided pyramids. Dektak 150 stylus surface profilometer is a thin film thickness measurement tool. An approach of measuring the textured surface pyramid heights by this tool is a new concept. It was analyzed by 2D graph of this profilometry. The Ideal value of pyramid height would be 3-5 micron where the findings shown 2.97 and 3.12 microns. The measurement technique was simple and easy. During the fabrication, one of the aims was to reduce the light reflection from the surface of silicon wafers. For this purpose it was later checked by Spectroscopic reflectometer and spectral reflectance measurement tools. From the initial to textured stages it has shown that light reflection was almost reduced to 50%.

4.8 References

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Chapter V

Fabrication and Characterization of Emitter Layer in Silicon Wafer

5.1 Introduction

In this chapter, the operation of the Atmospheric Pressure Chemical Vapor Deposition (APCVD) horizontal tube furnace and spin on doping mechanism is described. Phosphorus oxychloride ($POCl_3$) and P5O9 dopant solution were used as the n-type dopant material for mono-crystalline silicon substrate. This chapter also discuss about, required temperature, gas flow rate, APCVD chamber, steps for spin programming etc. For $POCl_3$ diffusion, nitrogen was used as carrier gas for safe operation though the pickup rate for material is independent of carrier gas. The instrumental details of the diffusion furnace, spinning tool and rapid thermal processing (RTP) furnace are discussed in Appendix I.

Various characterization techniques on the phosphorus doped samples is also discussed here. Before the characterization procedure start the important part is to isolate the p-n junction. The Phosphorus doped layer covers the entire surface including edges. So it is necessary to disconnect the front emitter from the back contact through etching the edges of the sample. Polarity and doping uniformity was measured by hot probe technique; where the details of in house made hot probe technique described before in chapter 3. SEM measurement shows the surface morphology. Energy dispersive x-ray spectroscopy (EDS) shows the elemental presence inside the sample. Percentage reflectivity was measured by spectroscopic reflectometer. Four point probe was used to measure the sheet resistivity of the doped sample. Anti reflection coating (ARC) layer thickness measured by spectroscopic reflectometer.

5.2 Thermal diffusion process

In solar cell fabrication, the emitter is formed by doping process. Doping refers to the addition of specific impurities to a semiconductor to modify its electrical properties. Moreover, there are two main methods of doping. They are: thermal diffusion and Ion implantation methods. Thermal diffusion can be performed with chemical vapor deposition technique. Chemical vapor deposition is a process, where gaseous reactants can be deposited onto a substrate [1].There are several types of CVDs, including low pressure chemical vapor deposition (LPCVD), atmospheric pressure chemical vapor deposition (APCVD), metal-organic chemical vapor deposition (MOCVD) etc. [2]. The Atmospheric Pressure Chemical Vapor Deposition (APCVD) chamber along with $POCl_3$, N_2, and O_2 gas, can grow an n-type emitter layer over Czmono-crystalline P-type silicon wafer. Doping also depends on various factors most importantly chamber temperature, selected gaseous environment with various flow rate, time etc.

The n-type dopant phosphorus oxychloride $POCl_3$ along with N_2 and O_2 gaseous environment is widely used in the standard diffusion process of solar cell fabrication. $POCl_3$ has low boiling temperature of 105.8˚C decomposed into phosphorus compounds like P_4, P_8, P_2O_5 etc. at temperature between 800-900˚C. These phosphorus compounds react with O_2 and create a glass layer on the silicon surface. The n-type doping element phosphorus then created at the glass and silicon interface and then penetrates into the silicon wafer. The penetration depends on temperature dependent diffusion coefficient [3,4].

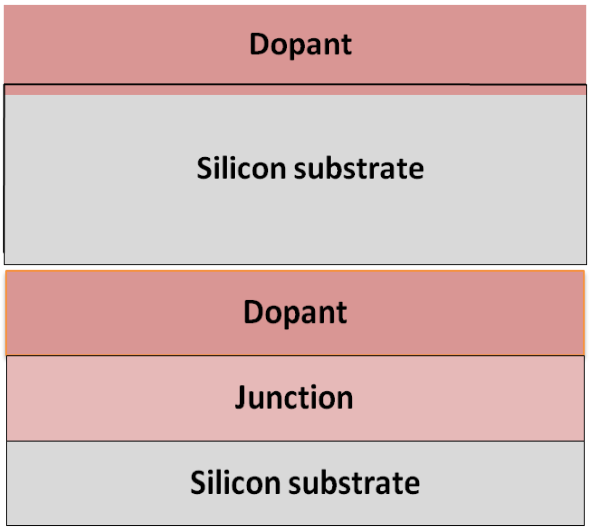


Figure 5.1 Illustration of thermal diffusion (a) pre-deposition (b) drive-in

The chemical reaction for the oxidation of the $POCl_3$ is as follows [3]

Pre-deposition:

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (5.1)$$

Drive in:

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (5.2)$$

At first, wafers were vertically placed into a quartz boat. For the n-type emitter formation onto the p-type silicon substrate the temperature of the quartz tube should be maintained at 800˚C to 900˚C. The quartz boat carrying silicon samples were moved into a horizontal quartz tube.

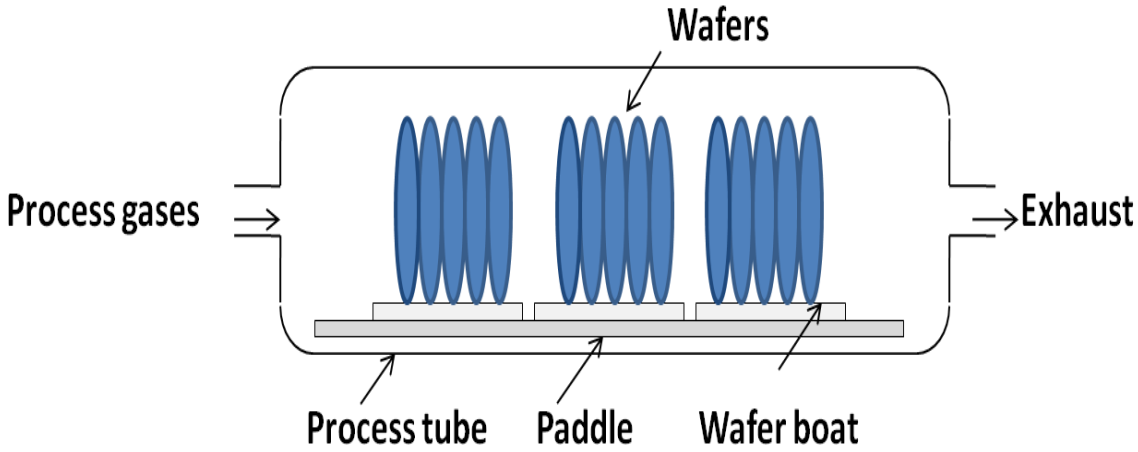


Figure 5.2 Wafer loading in the horizontal thermal diffusion system

The carrier N_2 gas flows through a bubbler that filled with liquid phosphorus oxychloride ($POCl_3$) and produces the gaseous $POCl_3$. The gaseous $POCl_3$ was mixed with O_2 and conducted directly into the heated quartz tube. Phosphorus oxide (P_2O_5) deposited onto the wafer surfaces in the pre-deposition stage. In the drive in stage phosphorus have been diffused into the silicon forming a p-n junction. The released Cl_2 removes metal impurities.

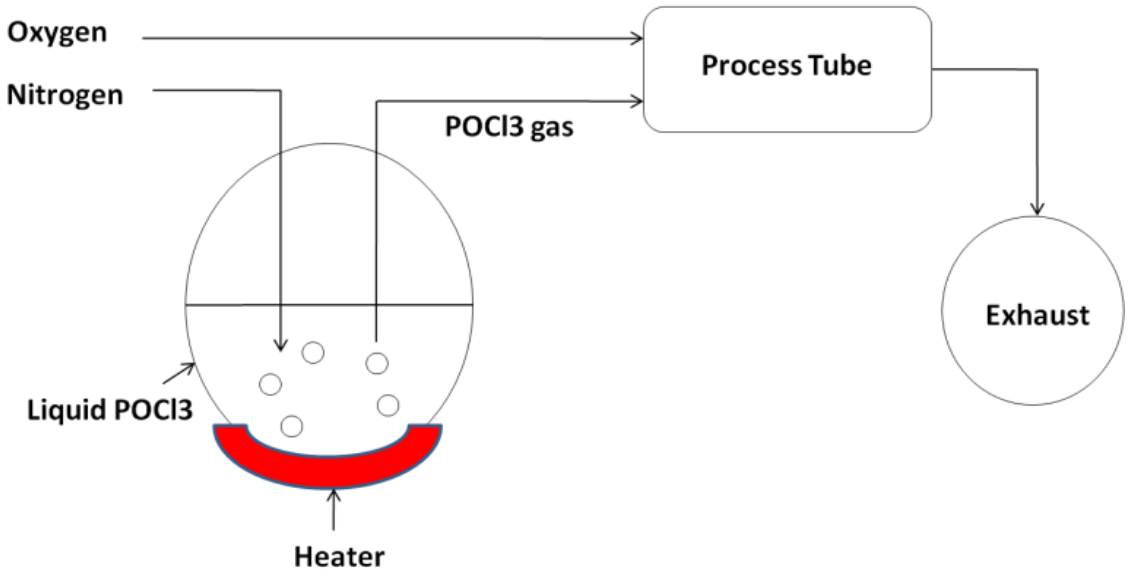


Figure 5.3 Bubbler system

5.2.1 Precautions before handling $POCl_3$

In this paper $POCl_3$ dopant has been used. It can cause serious and permanent eye injury. It causes skin burns that can be deep and poor in healing. If inhale it can cause lethal poisoning. It is toxic enough which causes serious damage to health by prolonged exposure if swallowed. For the precaution, try to remove or take off all contaminated clothing immediately. For the case of skin, rinse with water/shower. For the case of eyes, rinse cautiously with water for several minutes and remove contact lenses. For safety, keep the $POCl_3$ container tightly closed and dry places. Wear suitable protective clothing, gloves and eye/face protection. For extreme case, seek the medical advice immediately [5, 6].

5.2.2 Condition for $POCl_3$ diffusion

The first step is to determine the volume of the tube. The information of gas exchange rate will provide an adequate source of new material to the wafer surface. Divide the volume of the tube by using a gas exchange rate of every 3-7 minutes will give the information of main N_2 gas flow rate. The next step is to decide the O_2 flow rate. By using 5% of the main N_2 flow will give the information of oxygen flow rate. The source nitrogen flow will be the same percentage of the oxygen flow because one bubbler is used with fixed temperature [7].

The volume of the horizontal tube can be calculated by the following equation

$$V = \frac{\pi r^2 L}{1000} \quad \text{.....(5.3) [7]}$$

Where, V= total volume of the tube in liter

π= 3.1416

r = radius of the diffusion tube in cm

L = length of the diffusion tube in cm

The APCVD furnace containing three tubes was supplied from Sandvik's MRL phoenix with tube diameter 254 mm and length 1.22 meter for the supplied wafer of 125 × 125mm^2. The 2000cc bubbler was used at temperature of 20°C [8,9].

Calculated volume becomes 61.78 liter.

The standard value of gas exchange rate was chosen 5 minutes. Now divide the volume of the tube by the gas exchange rate and get the main nitrogen gas flow rate of 12.4 lit/min (SLM). The gas flow rate of O_2 and carrier N_2 gas into the bubbler was also calculated. These are shown in the table 5.1[7].

Table 5.1 Various gas flow rate for APCVD thermal diffusion

Gas name	Flow rate (lit/min)
Main N_2	12.4
O_2	0.62
Carrier N_2	0.62

$POCl_3$ pickup rate can be calculated by the following equations

$$M_{POCl_3} = \left[\frac{P_{vap}}{P_B - P_{vap}}\right].\left[(Q_{C2}).\left(\frac{MW}{22414}\right)\right] \text{.....(5.4) [7]}$$

Where M_{POCl_3}= $POCl_3$ Pickup Rate in grams per minute.

P_{vap}= $POCl_3$ Vapor Pressure (torr) at bubbler temperature

P_B= Bubbler pressure (760 mmHg or torr)

MW=Molecular weight of chemical ($POCl_3$=153.33 g/g-mole).

Q_{C2}=Carrier flow at SLM or sccm

P_{vap} could be chosen from the following graph shown in figure 5.4 for the bubbler temperature 20◦C [7]. $POCl_3$ Vapor Pressure was found 25 mmHg or torr.

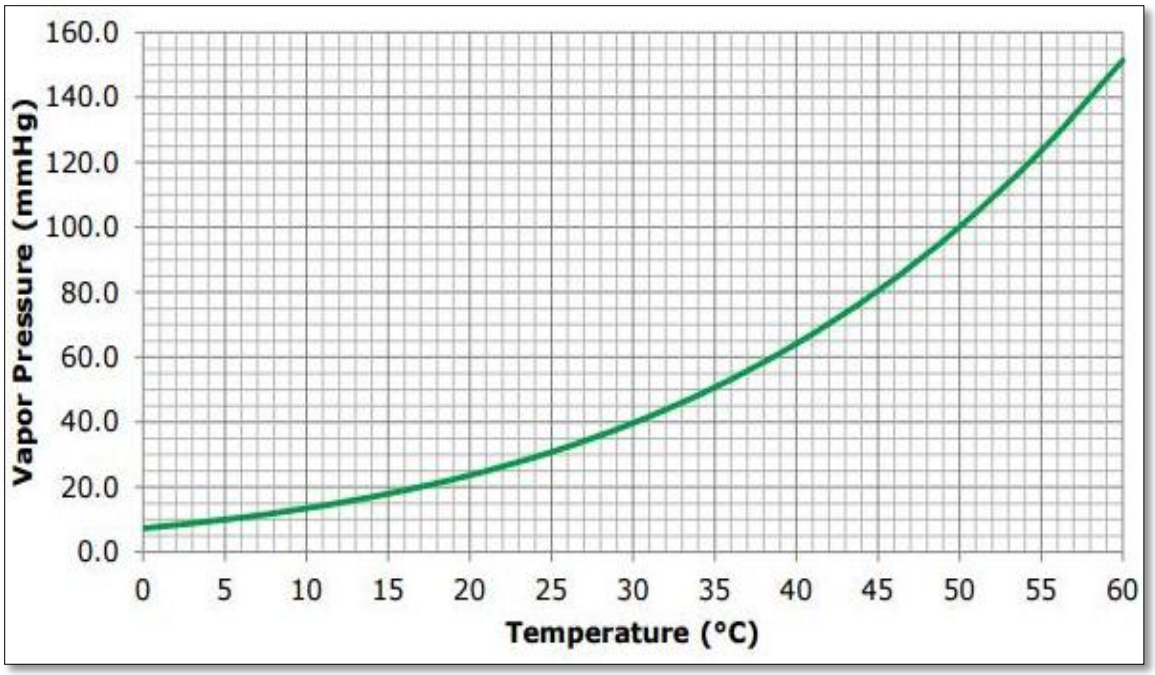


Figure 5.4 Graph for Bubbler temperature versus POCl3 vapor pressure [7]

For the carrier N_2 flow rate 620 sccm, calculated $POCl_3$ pickup rate is approximately 0.1476 g/min. The result of $POCl_3$ pickup rate is matched with the following graph shown in figure 5.5 [7].

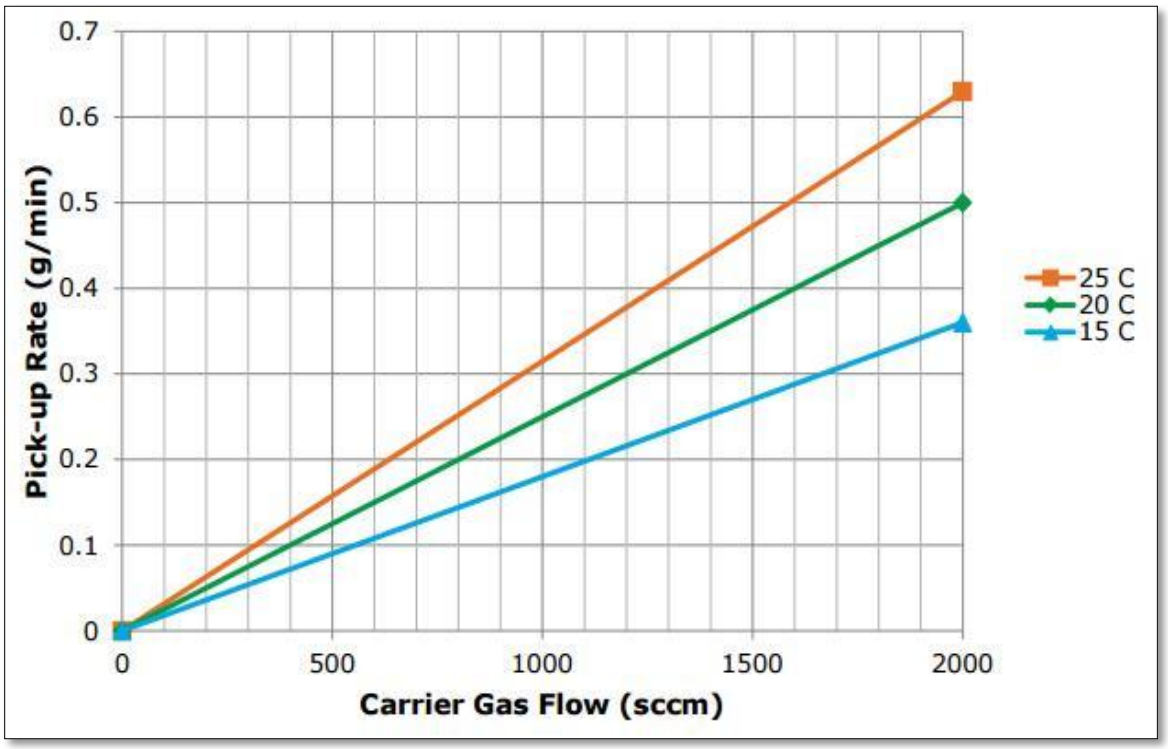


Figure 5.5 Graph for carrier gas flow versus pickup rate at three different bubbler temperatures [7]

5.2.3 Temperature dependent sheet resistivity

The doping causes the reduced sheet resistivity than the initial value shown in raw wafer. So by measuring the value of sheet resistivity one can easily understand the p-n junction is either formed. The solid solubility of Phosphorus (maximum number of active phosphorus atoms) in silicon material shows different values on various temperatures. In this work 875˚C temperature was chosen for $POCl_3$ diffusion. Temperature dependent number of active phosphorus atoms and the sheet resistivity is shown in the table 5.2.

Table 5.2 Temperature dependent solid solubility of phosphorus and the sheet resistivity for silicon sample [7]

Temperature (˚C)	Solid solubility of phosphorus in silicon (cm^{-3})	Sheet resistivity (Ω/sq)
850˚C	3.5×10^{20}	38-100
900˚C	5×10^{20}	15-40
950˚C	6.8×10^{20}	6-20
1000˚C	8.5×10^{20}	3-10

5.2.4 Operation and process time

At first, the $POCl_3$ furnace system was turned on. N_2 gas supply tank was turned on and set the flow at 75 PSI. If the pressure is low, raise it to 75 PSI and wait for the pressure gets stabilized. N_2 gas provides an inert environment, contamination and moisture-free diffusion chamber. O_2 gas supply tank, main circuit breaker switch, radio frequency heater power simultaneously turned on.

When the chamber temperature reached to 200°C turned on N_2 purge. After reaching 600 °C, the instrument was ready to load the wafers. The HF cleaned quartz boats hold the wafers that were placed on paddle and pushed the paddle slowly into the process tube. Note that the spacing between two wafers should at least 4.7 mm. When the temperature reached to 875°C, N_2 purge was turned off and N_2 source and O_2 source were turned on for 15 minutes. This stage is the pre-deposition process. After 15 min, N_2 and O_2 source were turned off by setting the flow meter to zero, and N_2

purge was turned on for 10 min for drive-in process. After completion of drive in process N_2 purge was turned off and O_2 source was turned on for 10 min for surface passivation. After that the O_2 source was turned off and N_2 purge was turned on for 10 minutes to have an inert environment, contamination and moisture-free diffusion chamber. During last N_2 purging, the temperature was lowered to 600°C and the wafers carrying paddle was pulled out from the chamber slowly. Quartz boats were collected and waited for 30 minutes for wafer cooled. Lastly, the temperature was lowered to 200 °C and the system was turned off.

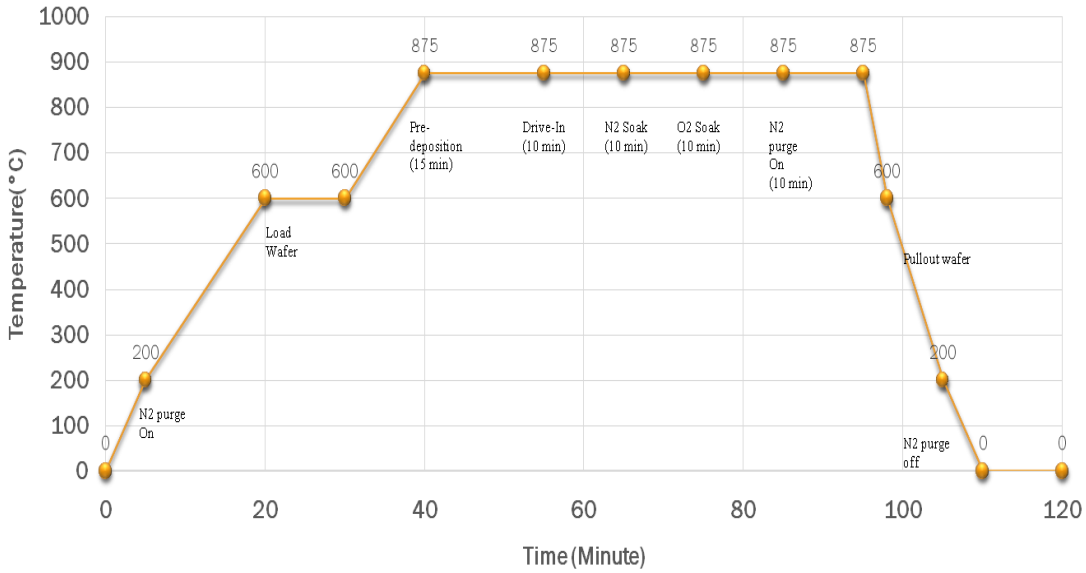


Figure 5.6 Temperature profile for growth of emitter layer by $POCl_3$ thermal diffusion

Figure 5.7 Image of in-house doped mono-silicon wafers

5.2.5 Single step for doping and surface passivation and ARC

Silicon nitride layer generally used to deposits on doped silicon surface by using plasma enhanced chemical vapor deposition. It is used to reduce optical losses and surface passivation [3]. In this thesis the thermal diffusion process is used for phosphorus diffusion as well as surface passivation and anti reflection coating by using an oxide layer deposit on doped silicon surface [10]. The refractive index of SiN is 2.0 where the refractive index of SiO_2 is 1.54. SiO_2 passivated layer may cause a very little effect on short circuit current density (mA/cm^2). But the advantage of this single step thermal diffusion process is to avoid the plasma-enhanced chemical vapor deposition tool. It reduces the fabrication cost as well as the reduction of silane and ammonia gases make the fabrication environment friendly.

5.2.6 Contamination control

To avoid any contamination it is necessary to use the clean room. Particle counter must be used inside the clean room before use. The paddle and the wafer carrying boat must be cleaned before use. The textured wafers have to be cleaned by HF before push inside the horizontal furnace. In this thesis, uniform N_2 gas flow has

been used for the contamination control during the thermal diffusion process. It also provides an inert environment and moisture-free diffusion chamber.

5.2.7 Challenges for Cl_2 gas removal

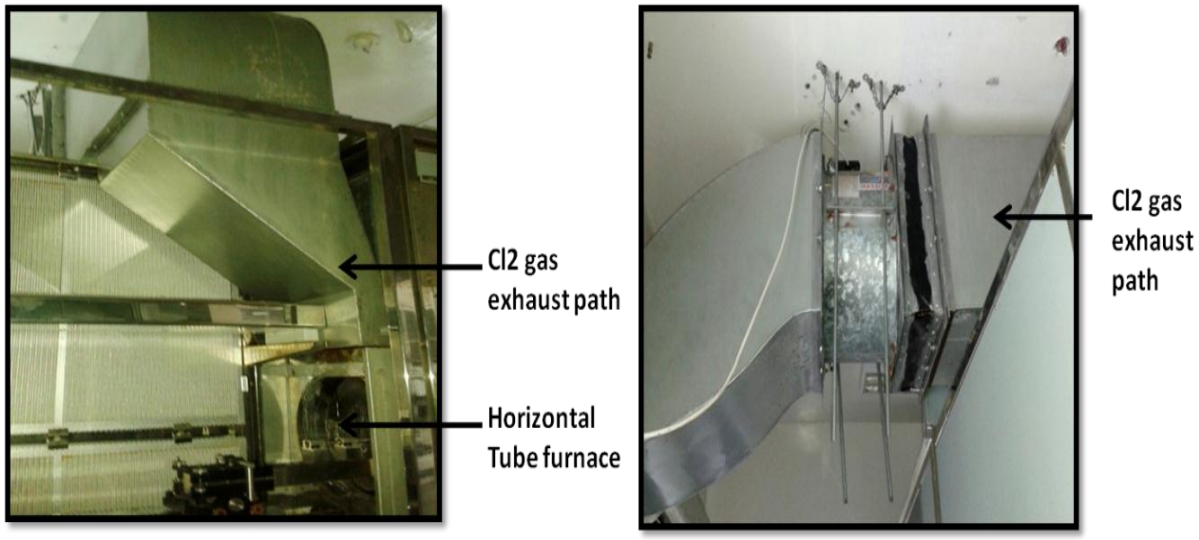


Figure 5.8 Cl_2 gas exhaust system

The exhaust in a furnace plays an important role on the diffusion process. The exhaust pressure determines the duration of stay of $POCl_3$ gas in the chamber. Also this makes the gas flow laminar over the length of the furnace which ensures uniform diffusion. An in house designed exhaust system was used in this case. The system maintains the exhaust pressure between 60mm of mercury. This implies that the exhaust provides required suction to take out all the gases from the furnace. At the end of the exhaust, a water shower was used that is why chlorine gas gets dissolved in water.

5.3 Spin-on process

Another way of doping by using the commercially available phosphorus doped oxide solution or spin on dopant (SOD) solution. It was supplied from Filmtronics Inc., PA, USA; P5O9 series [11]. This solution is high purity solution where phosphorous can diffuse into silicon with little or no surface damage. The surface concentrations after diffusion depend on the function of concentration of dopant in SiO_2 film. The P5O9 solution consists of 10% dopant compound and 5% of SiO_2 [11]. The concentration of phosphorous in P509 solution is 2.0×10^{21} cm^{-3}. This solution contains ethyl alcohol as a solvent and may be thinned with ethanol or

isopropanol to modify concentrations [11]. Note that the precise chemical compositions of the SOD solution are not disclosed by the manufacturer.

Several techniques such as spin on technique, spraying technique are available to produce SOD film on the silicon substrate [10]. In case of spin on technique, proposed spinning at 2000 to 6000 rpm to produce an oxide looking film [11]. Spinning of about 15-20 seconds is sufficient to provide uniform looking oxide film. Dopant would wet out uniformly over the surface of the silicon. After that the wafer is heated to 200°C for 10-15 minutes. During heating liquid solvents in the solution are evaporated and it takes the form of a solid film. After that the wafers are heated at 800-900˚C in the diffusion furnace with N_2:O_2 [3:1] environment for 10-15 minutes where phosphorus diffuse through the wafers [10, 12, 13].

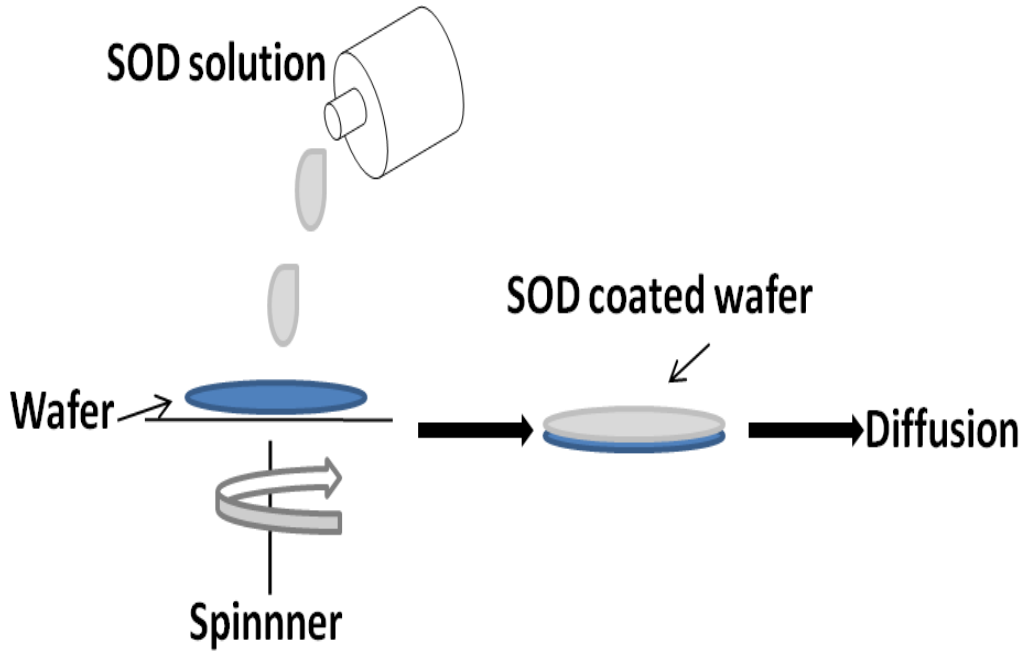


Figure 5.9 Spin on doping system

The drawback of spin coating is - it may cause some portion of the rear surface tend to be coated while front side corners may remain partially uncoated. Finally it is very difficult to identify the coating with bare eyes before heat treatment because the P5O9 solution is colorless. Spraying is another deposition method to cover the textured wafers. But the drawback is the acidic nature of the P5O9 solution may corrode metallic parts of the spray equipment [10, 11, 12, 13].

5.3.1 Precautions before handling P5O9

P5O9 SOD solution is not much toxic than $POCl_3$. While diffusion by $POCl_3$, chlorine gas produced as an exhaust gas which is necessary to filter out by a suction chamber and dissolved into water before it leave into environment. P5O9 solution may produce skin irritations or eye burns. Goggles can protect the eye burn. If the liquid or mist comes in contact with the skin or eyes the primary treatment is immediately wash with water for at least 15 minutes. Appropriate ventilation should maintain during spin on deposition [11].

5.3.2 Operation and process time

5.3.2.1 Film grown by spin coater

The SPS Spin 150 spin coater was used in this work [14, 15, 16]. Two step programming had done by this tool for P5O9 solution onto the silicon substrate by spin on technique.

The initial parameter and solution quantity selection are given below-

- Number of programming steps- 2
- Dopant solution- 5 ml, where 2.5 ml solution for each steps
- Wafer size 2.2×2.2 cm^2
- Chosen rpm is 1000
- Total time 80 seconds

At first the wafer was placed on vacuum secured sample holder of the tool. In the first step, the target was to reach 500 rpm by 10 seconds with an acceleration of 50 R/sec^2 and hold it for 5 seconds. As soon as it reached to 500 rpm we put 2.5 ml of P5O9 solution by a dropper/ pipette onto the wafer.

In the 2^{nd} step, the target was to reach 1000 rpm from 500 rpm by 50 seconds with an acceleration of 10 R/sec^2 and hold it for 1000 rpm for 15 seconds. As soon as it reached to 1000 rpm, put the rest 2.5 ml of P5O9 solution by the same procedure onto the wafer. Figure 5.10 shows the two step program settings on SPS Spin 150 spin coater.

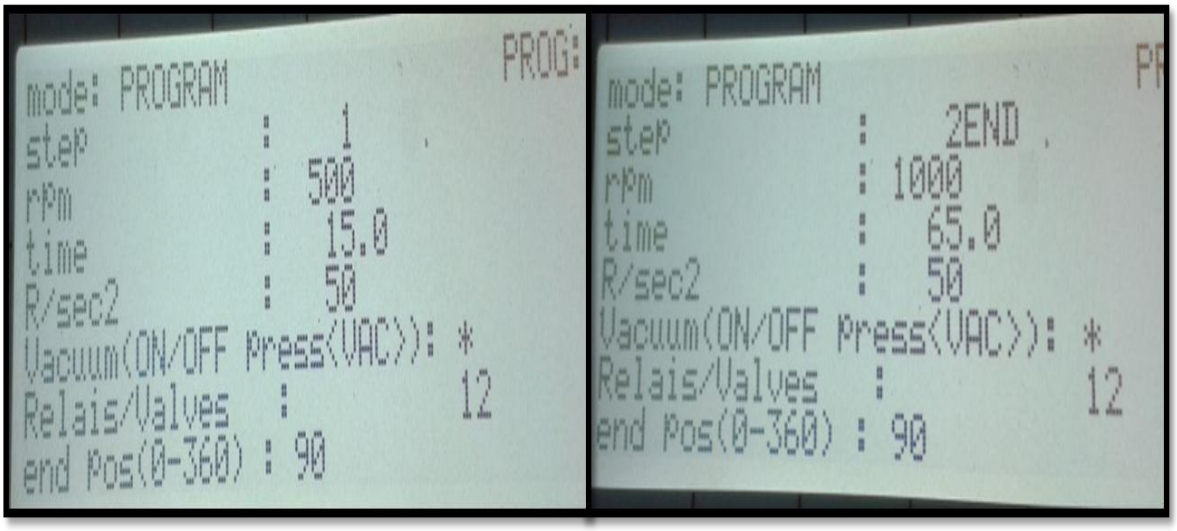


Figure 5.10 Two step program on SPS Spin 150 spin coater

rpm versus time profile for spin on process is shown in figure 5.11.

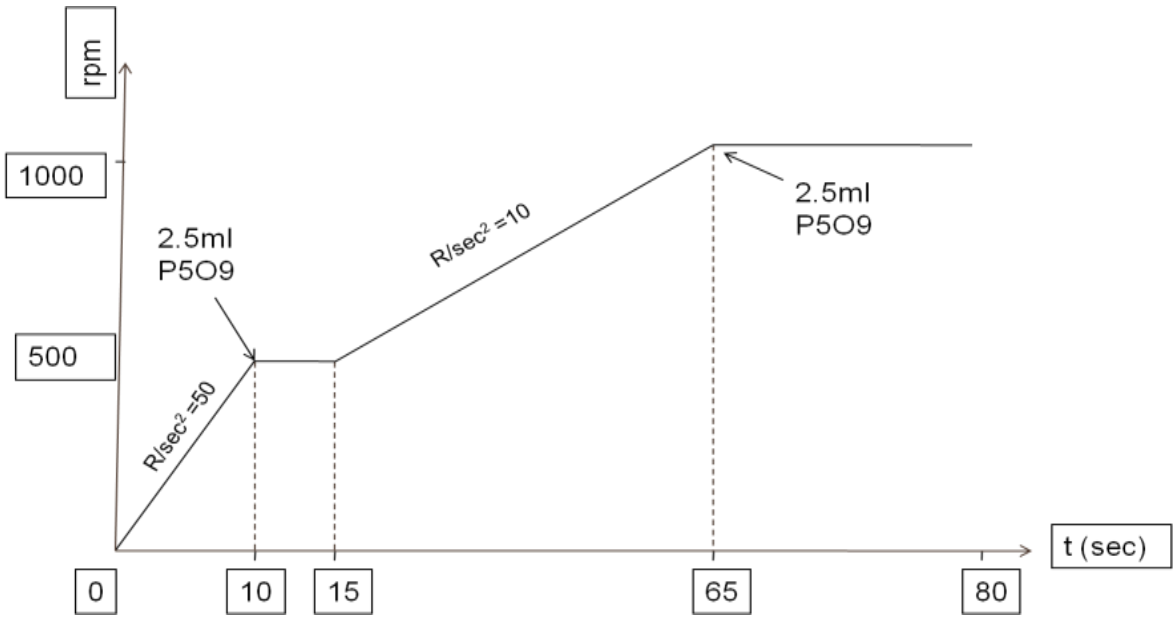


Figure 5.11 rpm versus time profile

5.3.2.2 Baking

After spin coating the wafers were prebaked at 200˚C for 10 minutes before they pushed into RTP chamber [11]. The hot plate from Fisher Scientific™ Isotemp™ with Ceramic Tops was used in this purpose (Appendix I-E). The liquid solvents (ethyl alcohol) were evaporated and the dopant solution forms a solid film.

5.3.2.3 Diffusion by RTP furnace

The RTP (rapid thermal processing) tube furnace from MTI Corporation OTF-1200 X was used to diffuse the dopant phosphorus into the silicon substrate. The instrument had 4" diameter and 12" length quartz tube with halogen light tube for heating element. It had also vacuum flanges, K type thermocouple and 30 programmable segments for precise control of heating rate, cooling rate and dwell time [17]. The diffusion was carried out at 875˚C for 10 minutes and 20 minutes with the N_2 environment. The chosen purified N_2 flow rate was 30 sccm.

Process timeline for diffusion inside the RTP tube furnace is shown in figure 5.12

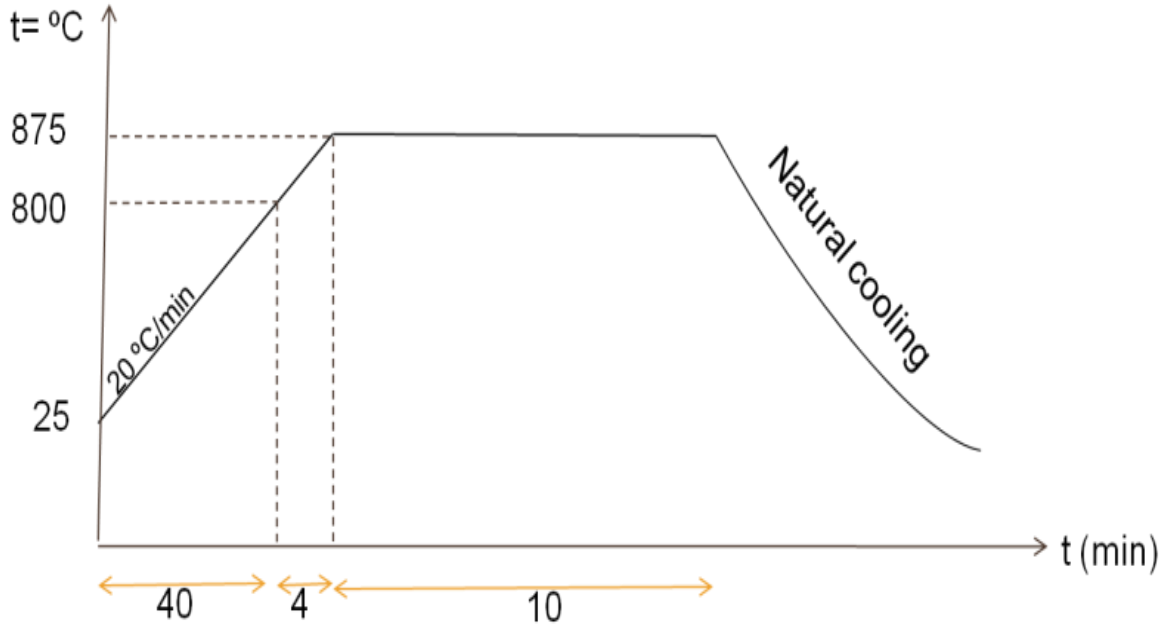


Figure 5.12 Time versus annealing temperature profile

Figure 5.13 Diffusion Process inside the annealing furnace

5.4 Dip coating by P5O9

In the case of spin on doping, SOD would wet out uniformly over the surface of the silicon. Spinning of about 15-20 seconds was sufficient to provide uniform looking oxide film [13]. But practically it might cause some portion of the corners on the front side remain partially uncoated. Finally it was very difficult to identify the coating with bare eyes before heat treatment because SOD solution (P5O9) was colorless. In this work, a manual way to cover the entire wafer by SOD solution has been used. The wafer was directly put into the P5O9 solution for 20-30 seconds and placed it inside the fume hood and waited for natural drying. After that wafers were put into RTP annealing furnace and diffused at a temperature 875˚C described in section 5.3.2.3. The process was very simple and easy and the uniform acceptable sheet resistivity was found.

5.5 Edge Isolation

The Phosphorus doped layer covers the entire surface including edges. It is important to disconnect the front emitter from the back contact through etching the

edges of the sample. Several processes are involved such as chemical etching, plasma etching, laser cutting, mechanical sawing, grinding with sand paper, single side etching etc. In this thesis single side etching and laser cutting techniques were used. For the single side etching, HF/HNO3 acid barrier paste was used. It was carried out by screen printing process. Samples were heated by 120ºC for 10 minutes by oven. Advantages of single side etching are preserving the active cell area, lower parasitic loss, higher FF compared to laser isolation process [3, 18].

Figure 5.14 Edge isolation mask screen

5.6 List of samples for diffusion process

In this chapter, three procedures of n-type emitter formation on p-type silicon substrate are discussed. The lists of samples are shown in table 5.3. Though p-type (100) mono-crystalline silicon sample of thickness 125 × 125 mm^2 was fabricated and characterized through the entire research, few work on other samples of different thicknesses and area have also used.

Table 5.3 List of samples: n-type emitter formation on p type silicon substrate using APCVD thermal diffusion, spin on doping and dip coating by SOD solution

Exp no.	Sample no.	Name of sample	Thickness	Area	Diffusion Process	Name of the laboratory
1	Sample-1	p-type (100), solar grade mono silicon wafer	180±20 µm	125 × 125 mm^2	APCVD thermal diffusion	Solar Cell Fabrication Laboratory, IE, AERE Savar, Dhaka
2	Sample-2	p-type (100), IC grade mono silicon wafer (single side polished)	600±50 µm	2.2 × 2.2 cm^2	dip coating by SOD solution	Thin Film Laboratory, SERI, UKM, Bangi, Malaysia
3	Sample-3	p-type (100), solar grade mono silicon wafer	180±20 µm	2.2 × 2.2 cm^2	spin on doping and dip coating by SOD solution	Thin Film Laboratory, SERI, UKM, Bangi, Malaysia

5.7 Properties of emitter layer in silicon wafer

5.7.1 Polarity measurement by hot probe

The hot probe set up was described before in the section 3.4. Initially type of the raw silicon wafers was tested by this experiment that was explained in the section 3.5. The same procedure was then applied for testing the phosphorus diffused wafer. The difference between the raw and the doped wafer would be the polarity difference of the developed potential across the voltmeter. In this case the voltmeter showed positive readings that determines the material was n-type.

The positive voltage reading determines the front emitter layer of the p-type wafer was converted to n-type layer. It also proved that the p-n junction was formed.

Table 5.4 Polarity measurement by using hot probe

Sample no.	Sample name	Diffusion Process	Voltage	Wafer type
Sample-1	p-type (100), solar grade mono silicon wafer	APCVD thermal diffusion by using $POCl_3$	11 mV	n-type
Sample-2	p-type (100), IC grade mono silicon wafer (single side polished)	dip coating by P5O9 SOD solution	0.1 V	n-type

5.7.2 Measurement of doping uniformity with hot probe

In order to fabricate an efficient solar cell it is important to know the doping uniformity of the emitter layer. The doping uniformity or wafer mapping can also be done by the hot probe measurement. In this procedure, the temperature was set first in the temperature controller then the 'Run' button was pressed and at the same time a regulatory knob of the hot plate was set low to high and then waited for few minutes to reach the predefined temperature 80˚C. Portion of sample-1 was placed on the hot plate where the rest was placed on a nonconductive base. Two k-type thermocouple placed simultaneously in contact with the hot and cold surface of the wafer to measure the temperature in situ for both hot and cold probe. The wafer began to heat up to 80˚C by the hot plate the thermally generated carriers started to diffuse from hot to cold portion. After few seconds the cold portion of the wafer simultaneously warmed up because of the diffusion of those heated carriers. So that, the built-in electric field tends to prevent the diffusion process and creates a steady state voltage. The steady state voltage is shown in figure 5.15 where it shows a dummy wafer of front and rear surfaces. In this situation, each measurement was taken by maintaining the probe distance 5 cm. The spacing between two measurements becomes 1.8 cm.

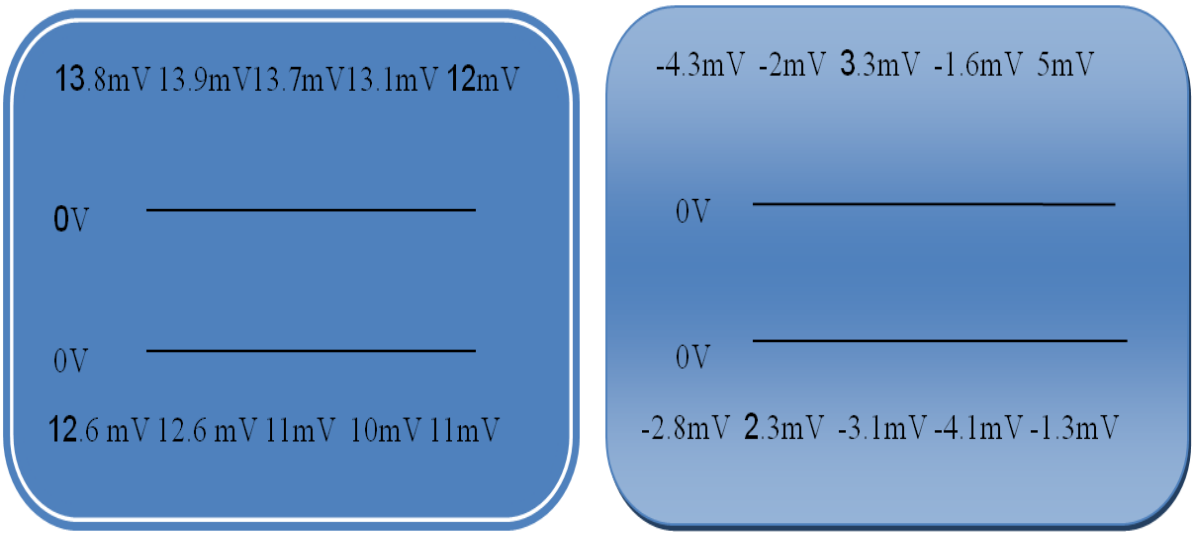


Figure 5.15 Doping uniformity measurements for sample-1 (a) front surface (b) rear surface

From figure 5.15 (a), it has shown almost uniform phosphorus doping. The average potential difference was +12.37mV throughout the front face of the wafer. That means after doping emitter layer was converted to n type. From figure 5.15 (b), it has shown the non uniform doping at the rear side. The average potential difference was +/- 2.98 mV throughout the rear surface of the wafer.

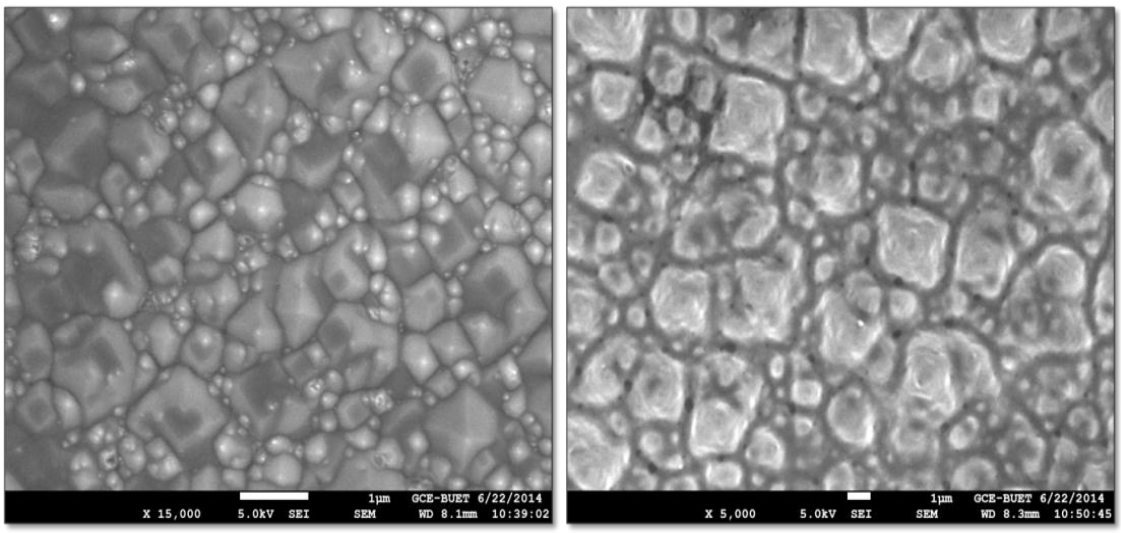
Table 5.5 Doping uniformity measurement by hot probe

Sample no.	Sample name	Diffusion Procedure	Average potential difference	
Sample-1	p-type (100), solar grade mono silicon wafer	APCVD thermal diffusion by using $POCl_3$	Front surface: 12.37mV	Rear surface: +/- 2.98 mV

5.7.3 Surface topography by scanning electron microscope

The Field Emission Scanning Electron Microscope (FE-SEM) was used to characterize the surface topography. The image was produced by scanning the sample with a focused electron beam and detecting the secondary or backscattered electron. The image was taken with 5kV electron beam, close working distance 8.3 mm and normal incident electron beam on the sample surface [19, 20].

Figure 5.16 (b) shows the image of phosphorus doped silicon sample. The surface topography of textured silicon sample is also shown in 5.16 (a) for comparison. The result said that the entire pyramidal surface was covered by a layer after doping. This layer was called surface passivation by anti-reflection coating. The layer composition later checked by energy dispersive x-ray spectroscopy (EDS).



(a) (b)

Figure 5.16 Comparison between (a) textured and (b) phosphorus doped sample-1

5.7.4 Energy dispersive x-ray spectroscopy (EDS) analysis

EDS gives the X-ray spectrum emitted by a solid sample bombarded with a focused beam of electrons to obtain the elemental analysis. The fundamental principle is that each element has a unique atomic structure allowing unique set of peaks on its X-ray emission spectrum. All elements from atomic number 4 (Be) to 92 (U) can be detected in principle. Note that, not all instruments are equipped for 'light' elements (Z < 10). Qualitative analysis involves the identification of the lines in the spectrum and is fairly straightforward owing to the simplicity of X-ray spectra. Quantitative analysis (determination of the concentrations of the elements present) entails measuring line intensities for each element in the sample and for the same elements in calibration Standards of known composition. An appropriate X-ray detector can be used to detect the characteristic X-ray spectrum from the sample. Elemental identification can be performed by matching the experimental spectrum to known X-ray energies which is automatically done using appropriated software [21, 22].

Topographical observation of silicon sample was taken out using Field Emission Scanning Electron Microscopes (FE-SEM) from Zeiss Sigma series with EDS system. EDS system with 10 mm silicon drift X-ray detector (SDD) was used for compositional analysis of doped silicon sample [20]. An electron beam of 20 keV was used as excitation source. Intensity versus photon energy curve allows us to evaluate the elemental analysis of impurity doped silicon substrate. Silicon, phosphorous and the presence of oxide layer have been detected on sample-1 using EDS spectrum. Peak position was analyzed corresponds to O was 525 eV (Kα), Si was 1.739 KeV (Kα), P was 2.013 keV (Kα) respectively [23, 24].

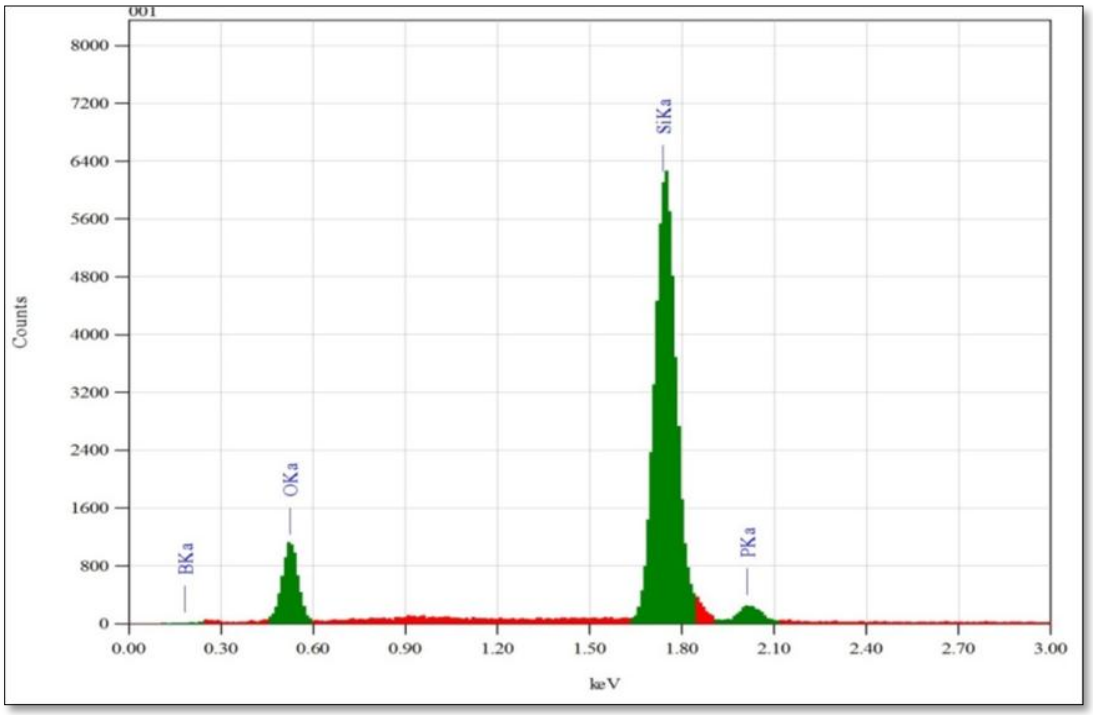


Figure 5.17 EDS spectrum of doped sample-1

Table 5.6 Compositional analysis using EDS

Sample no.	Name of sample	Diffusion Procedure	X-ray energy (KeV)	Element	Mass (%)	Atom (%)
Sample-1	p-type (100), solar grade mono silicon wafer	APCVD thermal diffusion by using $POCl_3$	0.525	Oxygen	25.87	38.14
			1.739	Silicon	68.86	57.84
			2.013	Phosphorus	5.28	4.02

5.7.5 Optical Reflectance

Optical reflectance of n-doped sample-1 had done by Spectroscopic reflectometer. The incident light falls normal to the sample surface so it is less expensive and much simpler than ellipsometry. This spectroscopy was used to check the percentage of light reflection from the sample surface. That is why it could compare among the samples during various fabrication steps. The function of spectroscopic reflectometer explained before in section 2.3.1.

The average reflectance factor is further reduced by SiO_2 surface passivation and anti-reflection coating. Figure 5.18 shows the comparative reflectivity changes graphs of textured and ARC coated doped silicon sample. The % reflectivity was reduced value than textured sample by an amount of almost 0.25% (650-800 nm). Note that the textured sample had the value of almost 1% (650-800 nm).

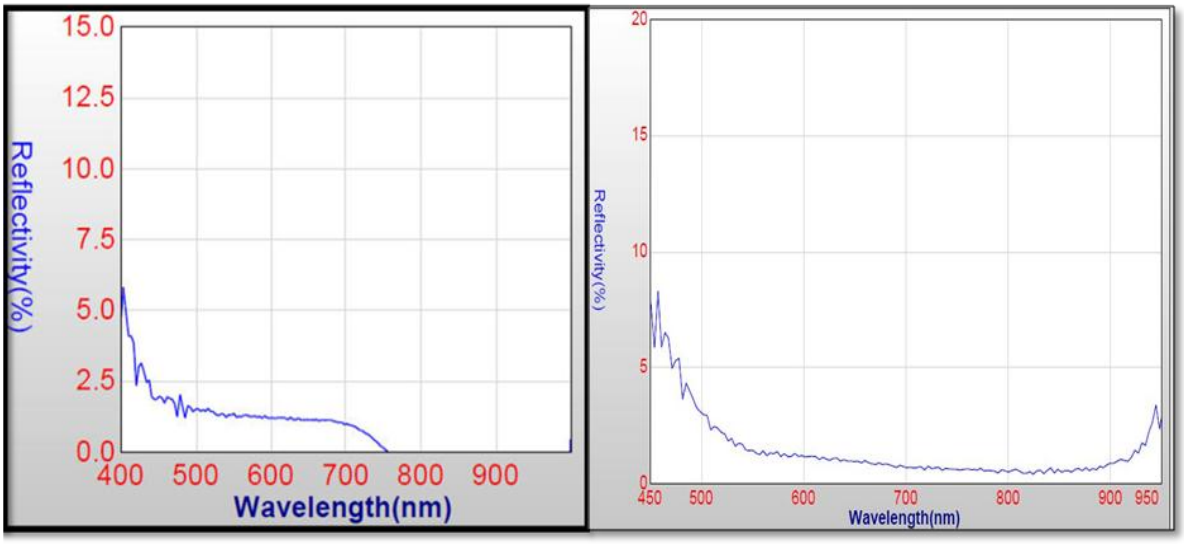


Figure 5.18 %Reflectivity versus wavelength graph for sample-1 (a) Textured silicon sample (b) doped silicon sample

5.7.6 Resistivity by four point probe measurement

The four point probe apparatus is one of the standard apparatus for the measurement of resistivity of semiconductors. When the sample is in the form of a thin wafer or the form of a thin semiconductor material deposited on a substrate it is useful for measurement.

Table 5.7 Measurement of sheet resistivity for doped sample using four point probe

Sample no.	Name of sample	Sample size	Diffusion Process, temperature and time	Sheet resistivity of raw sample	Sheet resistivity of n-doped wafer
Sample-1	p-type (100), solar grade mono silicon wafer	125×125 mm^2	$POCl_3$; 875˚C; 10 minutes	114.81 Ω/□	60 Ω/sq
Sample-2	p-type (100), IC grade mono silicon wafer (single side polished)	2.2×2.2 cm^2	P5O9; (a) 875˚C; 10 minutes (b) 875˚C; 20 minutes	145 Ω/sq	(a) 61.65 Ω/sq (b) 54.15 Ω/sq
Sample-3	p-type (100), solar grade mono silicon wafer	2.2×2.2 cm^2	P5O9; (a) 875˚C; 10 minutes (b) 875˚C; 20 minutes	141.41 Ω/sq	(a) 57.68 Ω/sq (b) 43.68 Ω/sq

5.7.7 Measurement of thickness

There are two types of procedure involved to measure the thin film thickness one is spectral reflectance and the other is ellipsometry. Spectral Reflectance measures the amount of light reflected from a thin film over a range of wavelengths, with the incident light normal to the sample surface.

To determine the film's thickness, the SR software calculates a theoretical reflectance spectrum that matches as closely as possible to the measured spectrum. It begins with an initial guess for what the reflectance spectrum should look like, based on the nominal film stack. This includes information on the thickness and the refractive index of the different layers and the substrate that make up the sample. The theoretical reflectance spectrum is then adjusted by adjusting the film's properties

until a best fit to the measured spectrum (Best-Fit-Algorithm) is found [25]. Spectroscopic reflectometer by Radiation Tech. Company Ltd. (Taiwan) was used for measuring the thickness of oxide layer. The oxide layer was deposited by using APCVD diffusion furnace during phosphorus doping.

Table 5.8 SiO_2 ARC film thickness measurement using spectroscopic reflectometer

Sample no.	Name of sample	Sample size	Diffusion Procedure	ARC film	Thickness (μm)	Refractive index
Sample-1	Solar grade mono silicon wafer	125×125 mm^2	APCVD thermal diffusion by using $POCl_3$	SiO_2	0.10126± 0.225092	1.455

5.8 Summary

In this chapter, the thermal diffusion process by using two different dopant solutions $POCl_3$ and P5O9 is explained. Three different procedures are: 1. APCVD $POCl_3$ thermal diffusion process 2. Spin on doping technique using P5O9 solution 3. Dip coating by P5O9 solution. All the three procedures carried out at 875˚C. As a large horizontal tube furnace for $POCl_3$ diffusion was used, there needed a large amount of N_2 and O_2 gases to complete the whole processes. But for spin on doping, the RTP chamber was small enough so that little amount of N_2 gases was used. Both diffusion furnaces are horizontal but the wafers were placed vertically for $POCl_3$ diffusion and horizontally for P5O9 diffusion.

Polarity measurement and an approach of doping uniformity measurement had done by hot probe. Surface topography clearly describes the passivated layer grown on silicon sample. EDS can measure the elemental presence in the sample. But not all instruments are equipped for 'light' elements ($Z < 10$). So that it couldn’t show the presence of boron inside the sample. Note that the raw sample was p-type boron doped silicon. The percentage of reflectivity of the doped sample was checked by Spectroscopic reflectometer (SR) tool. The value was shown little bit lower than the textured silicon sample. This result gave the idea that the surface was coated and

passivated. The resistivity was checked by four point probe. Note that if the diffusion temperature is fixed but diffusion time increases then it decreases the value of sheet resistance. The thickness of ARC coated SiO_2 layer was measured by spectroscopic reflectometer (SR) tool. The measured thickness was 0.101 μm.

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Chapter VI

Measurement for Carrier Lifetime and Conversion Efficiency

6.1 Introduction

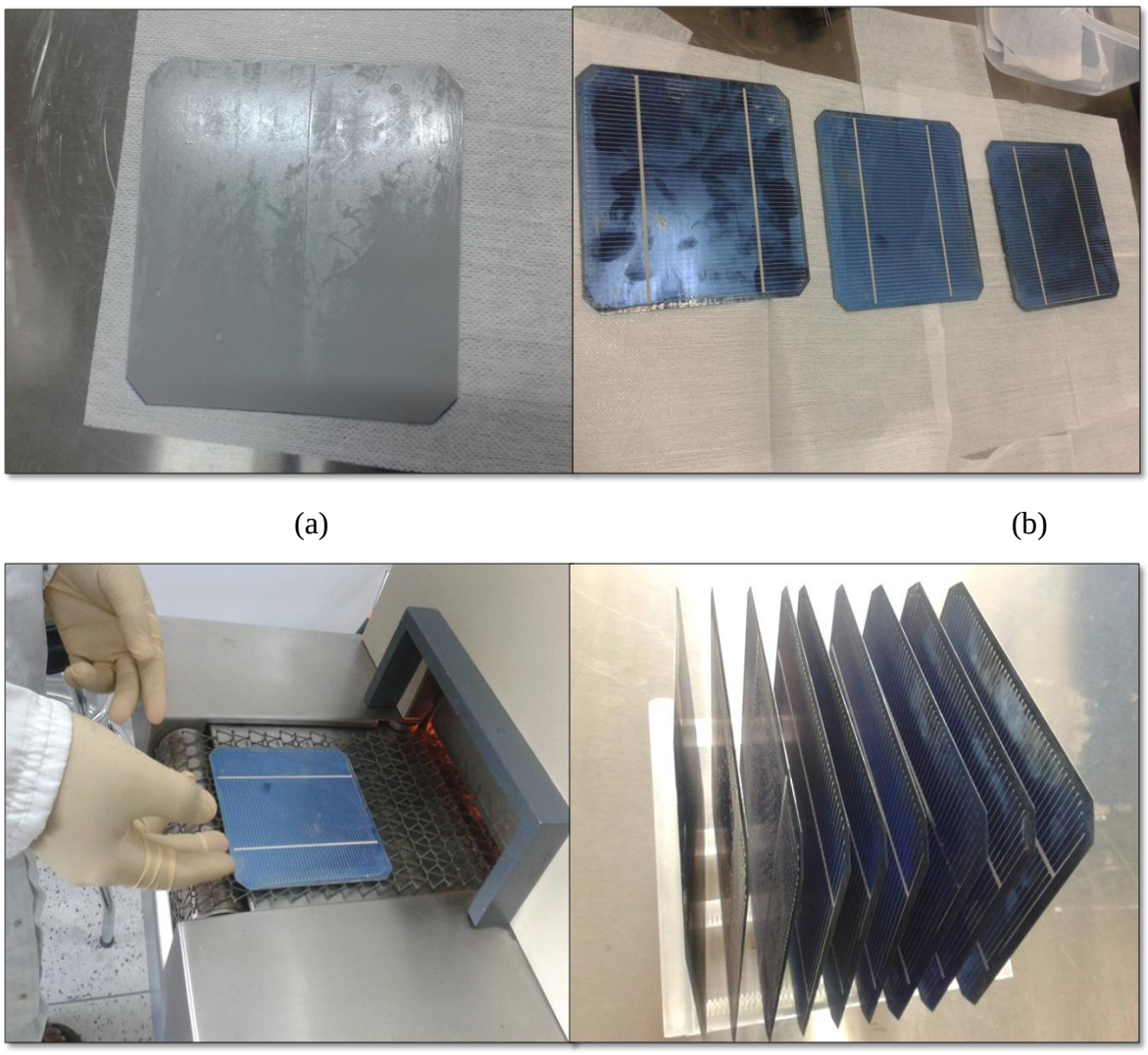
In this chapter, metallization and co-firing process is described before characterization for the completion of fabrication process. Minority carrier diffusion length through surface photovotage (SPV) technique has been measured. Minority carrier lifetime was then calculated from the minority carrier diffusion length. Total carrier generation and recombination during illumination can also be calculated using minority carrier diffusion length and the short circuit current density of the complete solar cell. Graphs are plotted by Microsoft Office Excel 07.

To reduce the cost it is important to reduce the cost of characterization tools for PV cells. For this purpose the solar simulators based on Xenon lamp light sources are most commonly used. These light sources are filtered optically to match the AM1.5G spectrum. It is an approach of reproducing the sun which is useful to characterize the PV cells. Basic parameters characterizing an IV curve are such as open circuit voltage (V_{OC}), short circuit current (I_{SC}), efficiency (η), and fill factor (FF). But the Xenon lamp based solar simulator has restricted lifetime, it cannot amend the spectral output, and generates a large amount of heat during the course of test illumination at one sun [1].

6.2 Metallization and co-firing

Before the I-V test the samples must go through the stages of metallization and co-firing. Back and front contact by using Ferro FX53-038 Al paste and Ferro CN33-462 Ag paste respectively were screen printed. Baking were carried out immediately after each metal printing step at 120˚C for 10 minutes. Wafers were co-fired by infrared lamp heated belt furnace with three different temperature zones

500˚C, 600˚C and 800˚C with the belt speed 40 inch/min (IPM). In the co-firing stage the metal electrodes penetrate through the wafer surface across the p-n junction.



(a) (b)

(c) (d)

Figure 6.1 (a) Screen printed rear surface by Al paste (b) Screen printed front surface by Ag paste (c) Co-firing process by belt furnace (d) Fabricated mono-silicon solar cell

6.3 Minority carrier diffusion length

The average distance that a carrier can move from the point of generation before recombination is called minority carrier diffusion length. Heavily doped semiconductor materials have greater recombination rates and have shorter diffusion lengths. Higher diffusion lengths means materials are of longer lifetimes and

improved quality. Diffusion length of semiconductor depends strongly on the type and magnitude of recombination processes. In silicon solar cells, Shockley read Hall (SRH) recombination is the dominant recombination mechanism. This recombination rate depends on the number of defects present in the material. Since doping increases the defects in the solar cell, hence that the rate of SRH recombination also increases. Auger recombination increases for heavily doped and excited material, which also enhances due to increase doping. Therefore we can say that the fabrication method and processing of a semiconductor wafer have a major impact on the diffusion length. For crystalline silicon solar cell the maximum carrier lifetime can be 1 millisecond and the minority carrier diffusion length is typically 100-300 μm [2, 3, 4].

6.4 Measurement of minority carrier diffusion length through SPV

In this work minority carrier diffusion length (L), and minority carrier lifetime (τ) was measured by contactless surface photovoltage technique. This technique changes the electrochemical potential in the space charge region of the solar cell. This changes causes by excess charge carrier generation due to illumination with the light of suitable wavelength and intensity. The distance that the photo generated carriers travel in the bulk before they recombine is called the minority carrier diffusion length. On a semiconductor whose spectral absorption coefficient is known, the minority carrier diffusion length can in principle be extracted from a measurement of photovoltage versus wavelength [2]. If we plot the light flux (Φ), divided by the SPV value (V_{SPV}) for each wavelengths, as a function of the penetration depth (reciprocal of absorption co-efficient) into silicon of those wavelengths, the result is a straight line which cuts X at its diffusion length L (0 to –X) [3, 5].

6.5 Carrier generation and recombination

The generation of an electron-hole pair is an important parameter; this is large at the surface of the solar cell, where the majority of the light is absorbed. The generation rate gives the number of electrons generated at each point of the material due to the absorption of photons. The light absorbed by a material depends on the absorption coefficient (α in cm^{-1}) and the thickness of the absorbing material. Light intensity at any point is given by

$$I = I_0 e^{-\alpha x} \quad \text{.....(6.1) [6]}$$

Where, α= absorption coefficient typically in cm^{-1}

x = distance into the material at which the light intensity is being calculated

I_0 =light intensity at the top surface

The above equation shows that the light intensity decreases exponentially throughout the material. This can also in turn be used to prove that the generation is highest at the surface of the material.

The loss of light intensity directly causes the generation of electron-hole pairs. The carrier generation *G* in a thin slice of material is determined by finding the change in light intensity across this slice. Consequently, differentiating the above equation will give the generation at any point in the material

$$G = \alpha N_0 e^{-\alpha x} \quad \text{.....(6.2) [6]}$$

Where, N_0= photon flux at the surface (photons/unit-area/sec.)

The incident light consists of many different wavelengths; for solar cell the generation rate at each wavelength is different. To calculate the generation of different wavelengths, the net generation is the sum of the generation for each wavelength. The front surface of a solar cell is at 0 μm where most of the high energy blue light is absorbed.

Again the recombination rate depends on the number of defects present in the material. As the doping increases the defects in the solar cell the rate of Shockley read Hall (SRH) recombination is also increases. It is the dominant recombination mechanism. Solar cell designers find the percentage of carrier generation and recombination in the three different layers emitter, depletion layer and base of the solar cell shown in table 6.1 [7].

Table 6.1 Carrier generation and recombination for emitter, depletion and base layer

Sample no.	Name of sample	Carrier	Emitter (%)	Depletion layer (%)	Base (%)
Sample-1	p-type, solar grade mono silicon wafer	Generation	0.37	0.14	0.49
		Recombination	0.75	0.02	0.23

Table 6.1 shows the heavily doped emitter is a low lifetime region. Because doping cause defects within the material. In the depletion region, the strong electric field swipes the carrier and collects them.

6.6 Quantitative derivation of carrier generation and recombination

When a photon hits the surface, in case of solar cell, electron-hole pairs are generated on the surface of the wafer due to energy transfer. The generation-recombination rate must be under control for the maximum output efficiency, i.e. that the carrier recombination rate must not exceed the carrier generation rate. The rate of recombination is the least at the junction region but increasing at the emitter and base region. Therefore the current must suffer in the solar cell due to uncollected generated current due to increased recombination; finally causing reduction of short circuit current (I_{SC}) and open circuit voltage(V_{OC}). For better understanding the relation between the recombination, generation of carriers has derived and took a quantitative approach in order to maximize the output.

Continuity equation for electrons become [6, 7]

$$\frac{\partial x}{\partial t} = -\nabla.\left(\frac{\overrightarrow{J_n}}{-q}\right) + G - R \text{……(6.3)}$$

At steady state, according to semiconductor equation conservation laws [6]

$$\nabla \cdot \vec{D} = \rho \text{ …… ….(6.4)}$$

Continuity equation for electrons equation (9.2) becomes

$$\nabla \cdot \left(\frac{\overrightarrow{J_n}}{-q}\right) = \left(G_{op} - R\right) \text{……(6.5)}$$

From Equation (6.5) we can write

$$\int_0^L dJ_n = q\int_0^L \left[R(x) - G_{op}(x)\right] dx \text{ ……(6.6)}$$

$$J_D(V) = J_n(L) - J_n(0) = q\int_0^L \left[R(x) - G_{op}(x)\right]dx = \quad q(R_{TOT} - G_{TOT}) \text{ …..(6.7)}$$

$$R_{TOT} = \int_0^L R\,(x)dx - \frac{J_p(0)}{q} - \frac{J_n(L)}{q} \text{ ……(6.8)}$$

$$G_{TOT} = \int_0^L G_{op}(x)\,dx \text{ ……(6.9)}$$

Dark current

$$J_D{}^{dark}(V_A) = qR_{TOT}{}^{dark}(V_A) \text{ ……(6.10) [7]}$$

Short circuit current (light generated current)

$$J_{SC} = J_D{}^{light}(0) = q\{R_{TOT}{}^{light}(0) - G_{TOT}\} \text{ ……(6.11)}$$

$$\text{And } J_{SC} = qG_{TOT}(L_n + L_p) \text{ ……(6.12)}$$

For electron

$$J_{SC} = qG_{TOT}(L_n) \text{……(6.13) [7]}$$

Where this L_n is the diffusion length for electron, D is the diffusivity, and τ is the lifetime [5]:

$$L_n = \sqrt{D\tau_n} \text{ ……..(6.14) [4, 7, 8]}$$

6.7 Experimental details

6.7.1 Minority carrier diffusion length

In the Surface photo voltage measurement system light comes from a tungsten-halogen lamp and focused into the entrance slit of the monochromator. The monochromator driven by a stepper motor can vary the wavelengths from 400-1200 nm spectral range. Monochromator output is guided to the solar cell at normal incidence. A chopper is placed at the exit slit of the monochromator to provide reference signal to the Stanford Research 510 lock-in amplifier to enhance system sensitivity from nano-volt to mV range. An ITO/Au coated quartz plate placed on the top of the solar cell. A thin-sheet of Teflon film is placed between the top glass electrode and the solar cell to create electrical isolation. The bottom electrode also connected to the solar cell and is Au-coated to provide reduced contact resistance. A Lab-view interface is used for data acquisition. The surface photovoltage vs wavelength data for mono crystalline silicon solar cell is plotted by Microsoft office excel 07 and shown in figure 6.2.

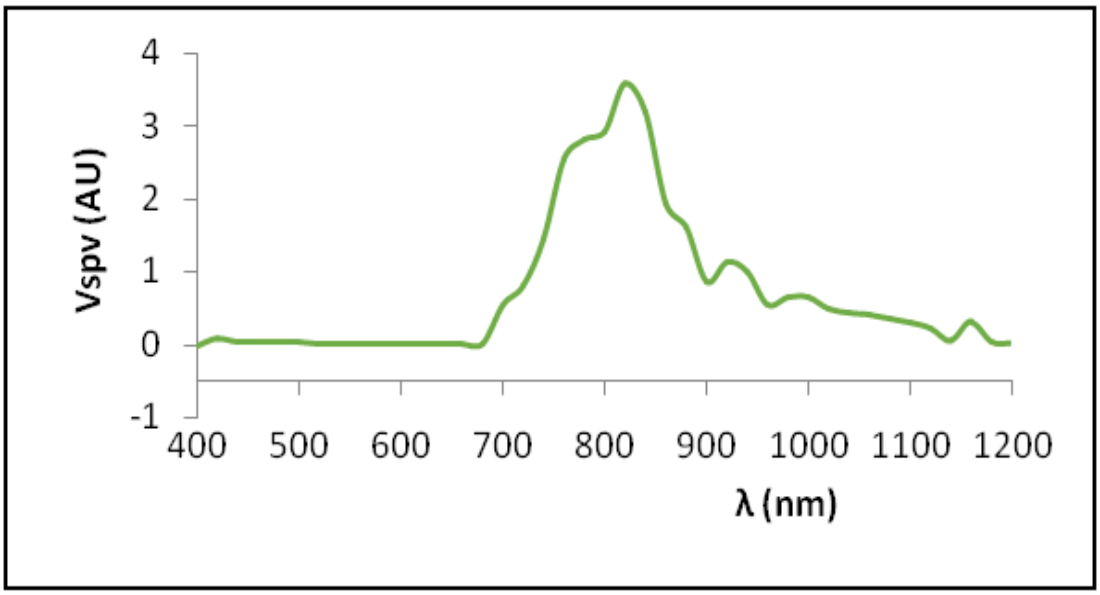


Figure 6.2 V_{SPV} versus wavelength (λ) graph: an output from the SPV measurement

In order to find the minority carrier diffusion length the first step is to plot the light flux (Φ) divided by the SPV data (V_{SPV}) for each wavelengths as a function of the light flux (Φ) divided by the absorption co-efficient (α) of silicon (Appendix- III) of those wavelengths. As the light flux (Φ) is common so it can be plotted the reciprocal of surface photovoltage ($\frac{1}{V_{SPV}}$) with respect to reciprocal of absorption co-efficient ($\frac{1}{\alpha}$) of silicon material. Note that the reciprocal of absorption co-efficient ($\frac{1}{\alpha}$) is called penetration depth into the silicon. The ($\frac{1}{V_{SPV}}$) vs ($\frac{1}{\alpha}$) data are plotted by Microsoft Office Excel 07 shown in figure 6.3.

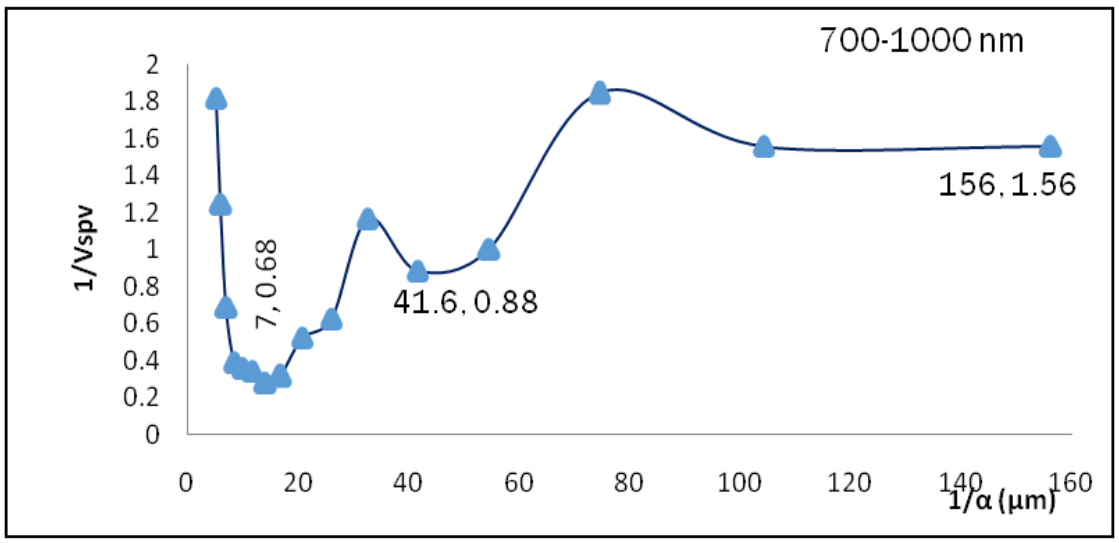


Figure 6.3 ($\frac{1}{V_{SPV}}$) versus ($\frac{1}{\alpha}$) graph

The 2nd step to find the minority carrier diffusion length, it needs to draw an average linear line which intersect at negative X axis. Another way is to select three data points between 700-1000 nm where the surface photovoltage shows the maximum values shown in figure 6.2 and draw a straight line that intersect the negative X axis. The average linear line or straight line that cuts at negative X is the value of diffusion length L (0 to –X) [3, 9]. Three data points from figure 6.3 for three different wavelengths between 700-1000 nm are shown in table 6.2.

Table 6.2 Penetration depth and $1/V_{SPV}$ with respect to wavelength

Sample no.	Name of sample	$\lambda\ (nm)$	$\frac{1}{\alpha}\ (\mu m)$	$\frac{1}{V_{SPV}}$
Sample-1	p-type (100), Solar grade mono silicon wafer	740	7	0.68
		920	41.6	0.88
		1000	156	1.56

Finally the value of minority carrier diffusion length (L_n) = 110 µm by drawing a straight line that cut at the negative X intersection was found that is shown in figure 6.4.

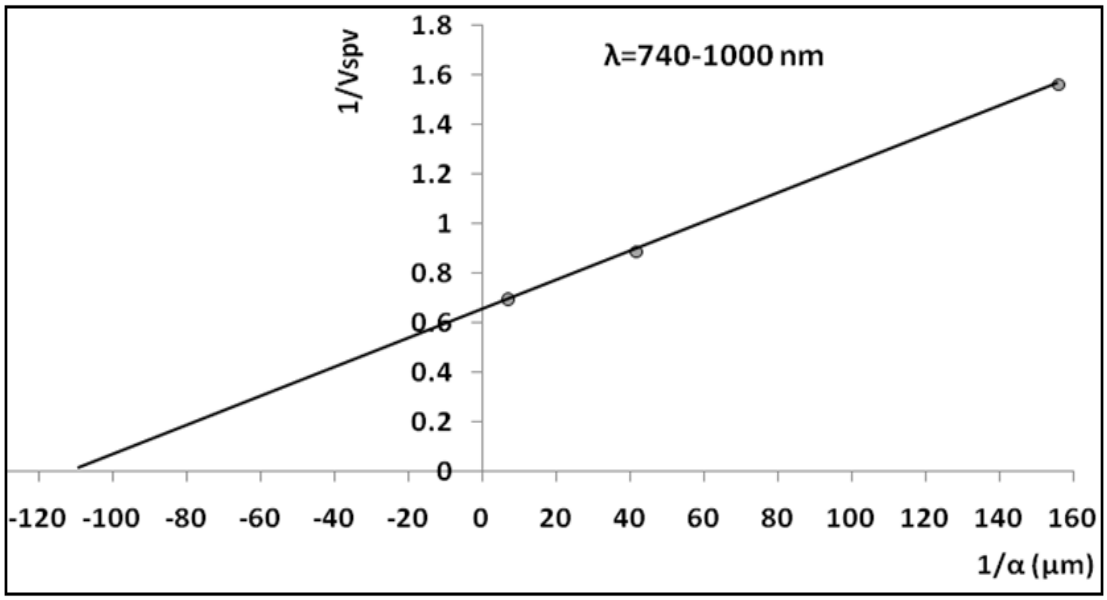


Figure 6.4 The straight line cut at -110 μm that gives the value of diffusion length

6.7.2 Minority carrier lifetime

Rewrite the equation (6.14)

$$L_n = \sqrt{D\tau_n}$$

Where, $L_n = 110\ \mu m$,

and $D = 27\ \frac{cm^2}{s}$

Then, $\tau_n = 4.48\ \mu s$.

Here τ_n is the minority carrier lifetime.

6.7.3 Carrier generation and recombination

Rewrite the equation (6.13)

$$J_{SC} = qG_{TOT}(L_n)$$

Where, the short circuit current density I_{SC}=18.1436 mA/cm^2

Carrier charge q= 1.602×10^{-19}

Minority carrier diffusion length L_n =110 μm

Then the calculated total carrier generation, G_{tot}= 1.0296E+18 /cm^{2}s

The percentage of carrier generation in the three different layers of sample-1 can be found with the help of table 6.1. Table 6.3 and figure 6.5 shows the carrier generation inside sample-1 [7].

Table 6.3 Carrier generation for emitter, depletion and base layer

Carrier generation			
G_{tot} (/cm^2s)	Emitter (37%)	Depletion Region (14%)	Base (49%)
1.0296E+18	3.80952E+17	1.44144E+17	5.04504E+17

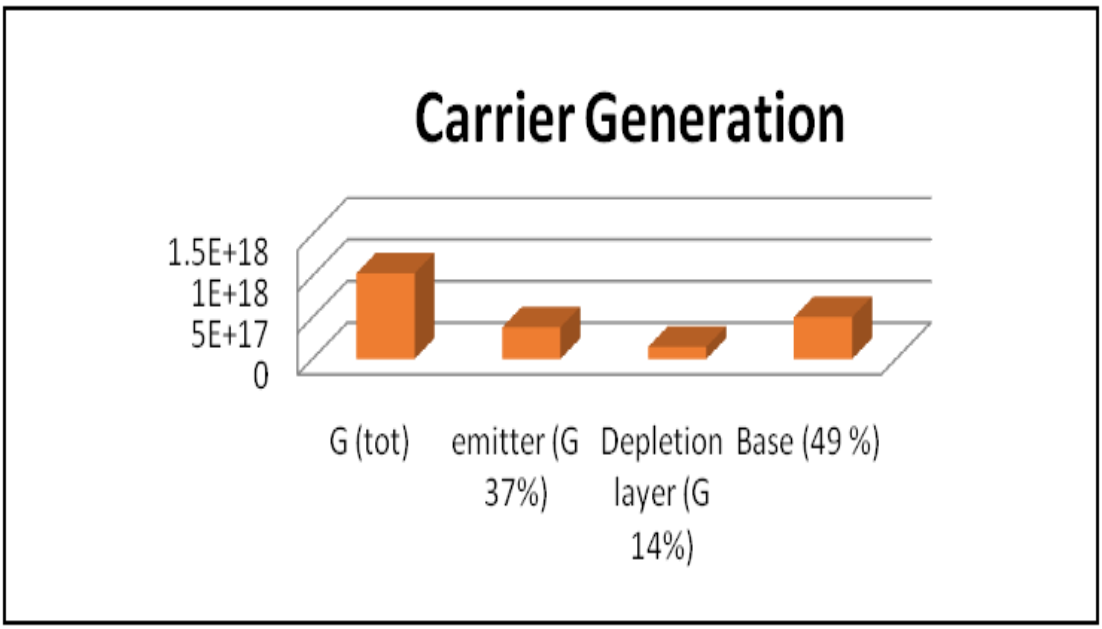


Figure 6.5 Carrier generation for sample-1

The percentage of carrier recombination in the three different layers of sample-1 can be found with the help of table 6.1 and the total carrier recombination are the sum of those values that are shown in table 6.4.

Table 6.4 Carrier recombination for emitter, depletion and base layer

Carrier recombination			
R_{tot}(/cm^2s)	Emitter (75%)	Depletion Region (2%)	Base (23%)
4.04633E+17	2.85714E+17	2.88288E+15	1.16036E+17

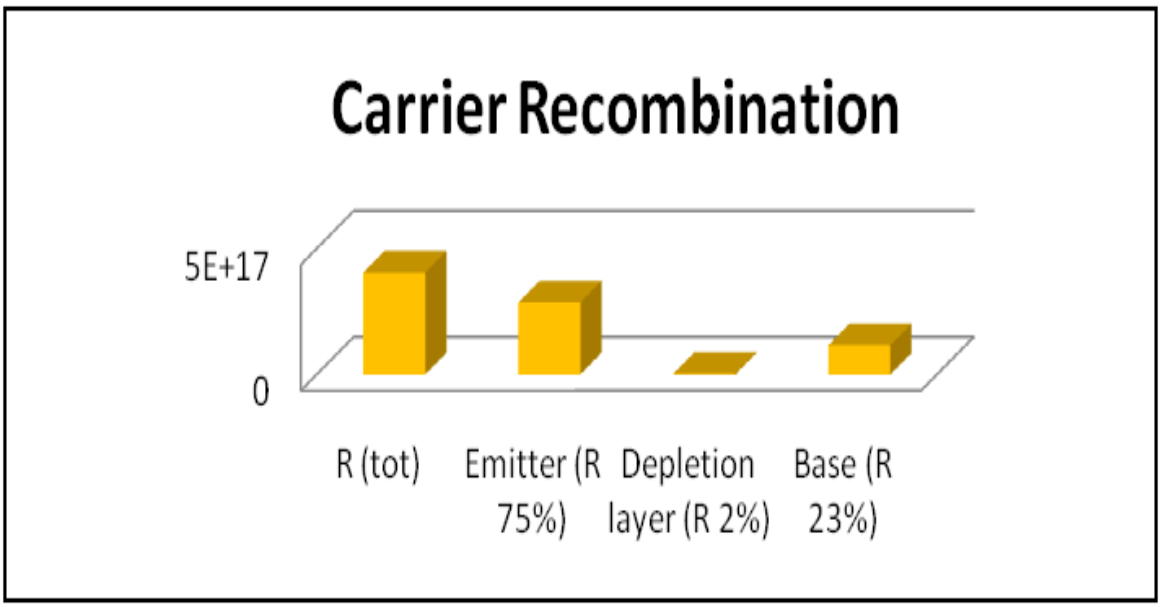


Figure 6.6 Carrier recombination for sample-1

The remaining carrier inside the solar cell can be found by subtracting the carrier recombination from the carrier generation with the help of table 6.4 and 6.3 respectively.

Table 6.5 Remaining carrier for emitter, depletion and base layer

Sample no.	Emitter	Depletion Region	Base
Sample-1	9.5238E+16 /cm^{2}s	1.41261E+17 /cm^{2}s	3.88468E+17 /cm^{2}s

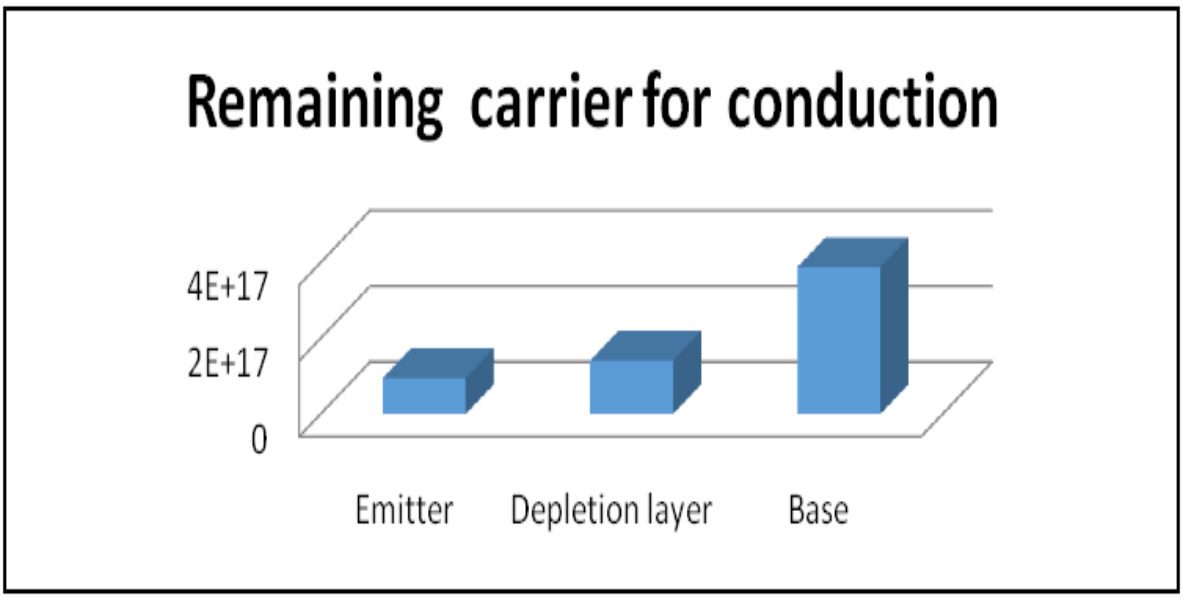


Figure 6.7 Remaining carrier for sample-1

For the total wafer thickness the carrier generation rate and recombination rate is calculated with the help of equation (6.6) and (6.7) divided by its dimensions. This can also be expressed by differentiating the equation mentioned. The final graphs obtained for generation and recombination rate is shown in figure 6.8.

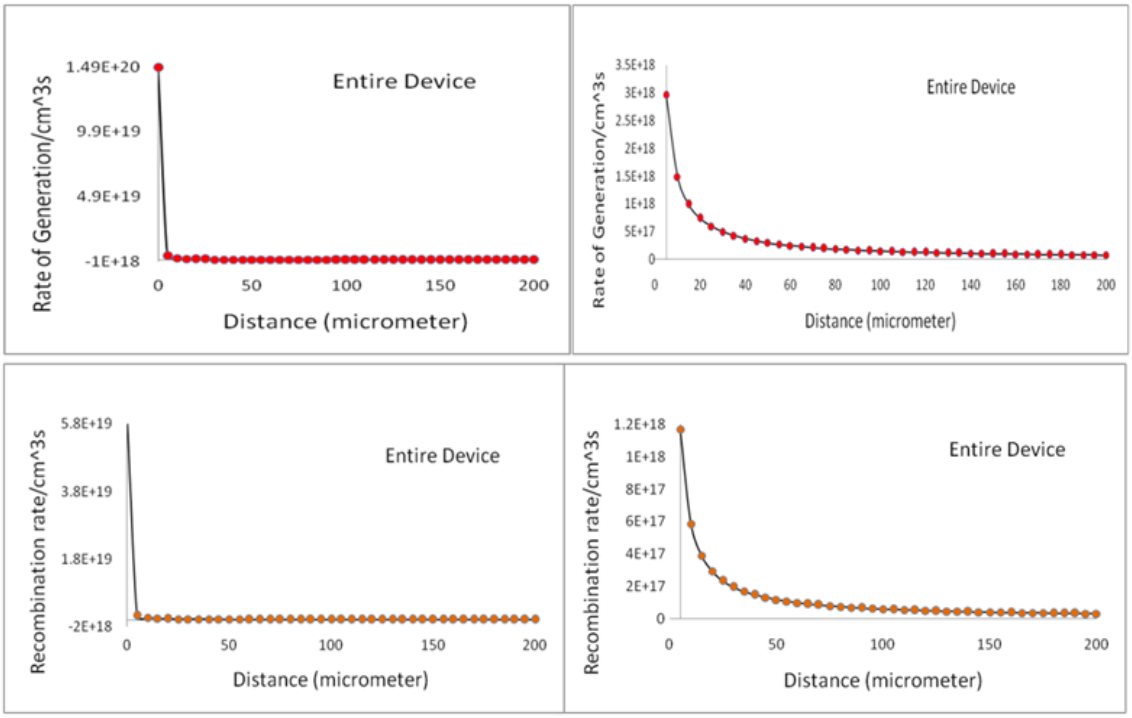


Figure 6.8 Total carrier generation and recombination rate for the entire thickness of sample-1 solar cell (left) and rest of the cell ignoring the surface (right)

6.8 Equivalent circuit for solar cell

PV cells are large PN junctions that produce electricity when light absorption imparts energy to individual electron hole pairs inside a cell. When there is no light, a PV cell can be designed as a current source along with a diode. In a voltage or current characteristic (IV), produced by a voltage sweep of a diode with a source meter, the current is exponentially associated with an applied voltage. Figure 6.8 shows a simple, similar circuit model for a PV cell that uses the model described above, together with extra series and parallel shunt resistance [10].

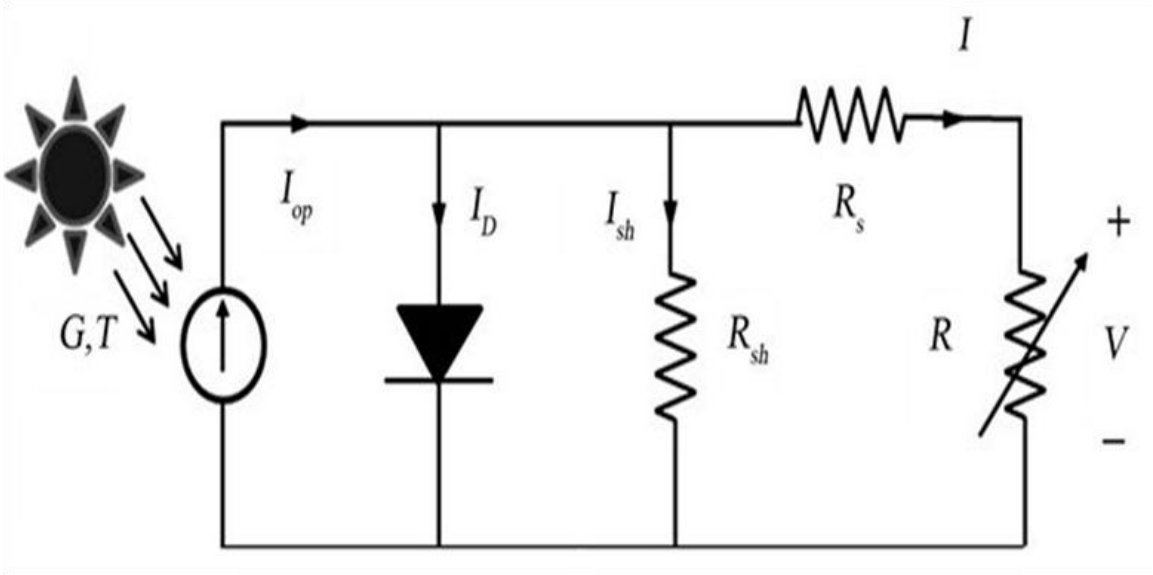


Figure 6.9 A diode circuit model describing a PV cell connected to a source meter for IV testing

Illuminated characteristics are merely the dark characteristics shifted down by a current I_L. This gives a region of fourth quadrant of this plot where power can be extracted from the diode. The light generated current I_L has a value equal to that expected if all the carriers generated by light in the depletion region of the diode and within a minority carrier diffusion length on either side were to contribute to it. The depletion region and the generally much larger volume of material lying within a diffusion length of either side of it is indeed the active collection region of a p-n junction solar cell. Three parameters are usually used to characterize solar cell outputs. First one is the short circuit current I_{SC}. Ideally I_{SC} is equal to the light generated current I_L. The second parameter is the open circuit voltage V_{OC}. Setting I equal to zero in the following equation the ideal value can get.

$$I = I_0 \left(e^{qV/kT} - 1\right) - I_L \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(6.15)}$$

V_{OC} is determined by the properties of the semiconductor by virtue of its dependence on saturation current density (I_0). The power output of any operating point in the fourth quardrant is equal to the area of the rectangle indicated in figure 6.10. One particular point (V_{mp}, I_{mp}) will maximize this power output [11].

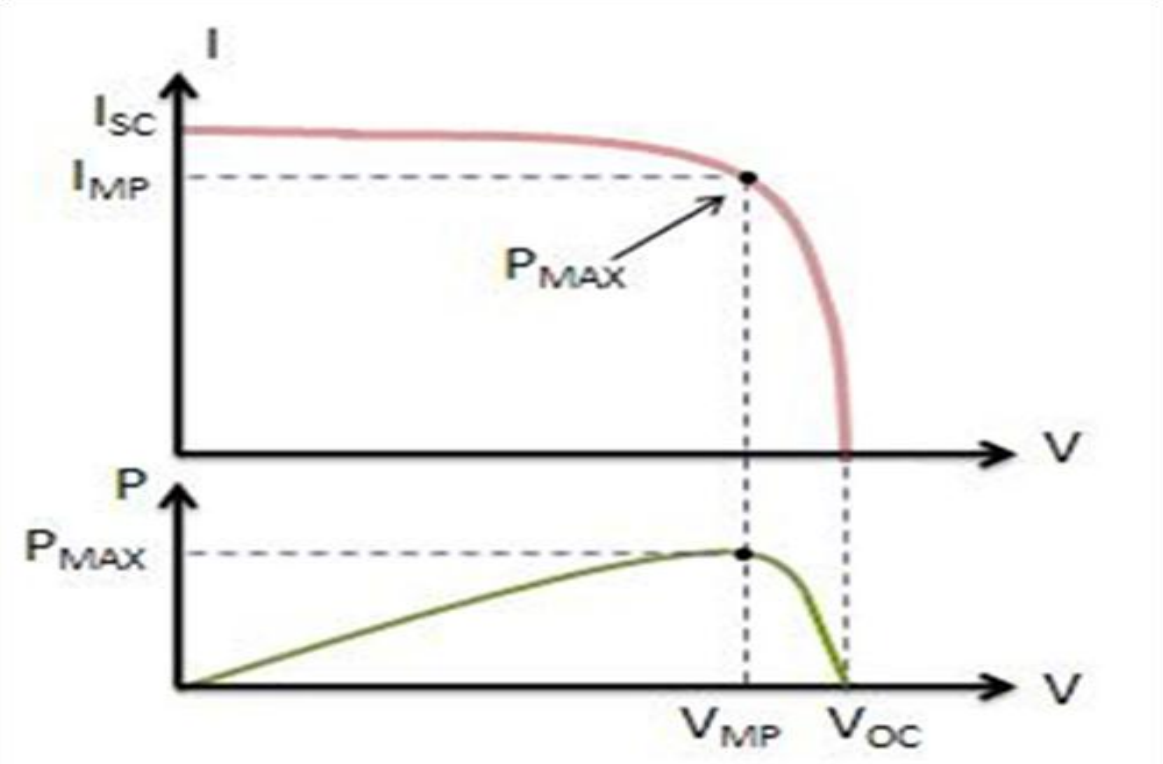


Figure 6.10 IV curve for a silicon PV cell

The third parameter is the fill factor is defined as

$$FF = \frac{V_{mp} I_{mp}}{V_{oc} I_{sc}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(6.16)}$$

It is a measure of how square the output characteristics are. Ideally it is a function of the open circuit voltage V_{OC} only.

The energy conversion efficiency □ is then given by

$$\square = \frac{V_{mp} I_{mp}}{P_{in}} = \frac{V_{oc} I_{sc} FF}{P_{in}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(6.17)}$$

Where, P_{in} is the total power of the incident light [12].

6.9 LIV setup for measurement

LIV tester is supplied by Gratings Inc. LIV measurements are based on pulsed xenon arc lamp as the illumination source. The system is capable of measuring solar cells in wide range of sizes varying from few cm^2 to ~ 180 cm^2. The light intensity varies from ~ 50 mW/cm^2 to 150 mW/cm^2; AM 1.5 is ~ 100 mW/cm^2. Specific features of this instrument includes-

i. Custom-designed current-voltage probes

ii. Programmable current-voltage measurement power supply

iii. Vacuum plate for holding wafers

iv. LabVIEW-based PC interface

and

v. Calibrated solar cells provided for system characterization.

Figure 6.11 (a) Custom designed probes (b) Programmable current-voltage measurement power supply with LAB VIEW based interface

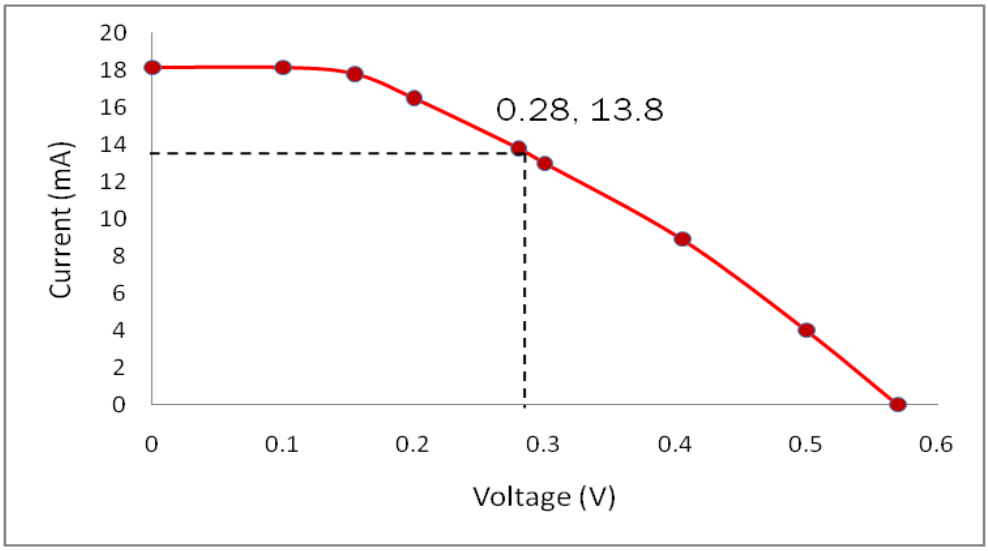
6.10 Measurement of conversion efficiency

LIV Measurements took at an intensity of 1 sun (1000 W/m) with the spectral match of AM1.5G. Temperature is a major issue because the lamp emits heat, which is transferred onto the sample so that, the measurement was taken in a fraction of

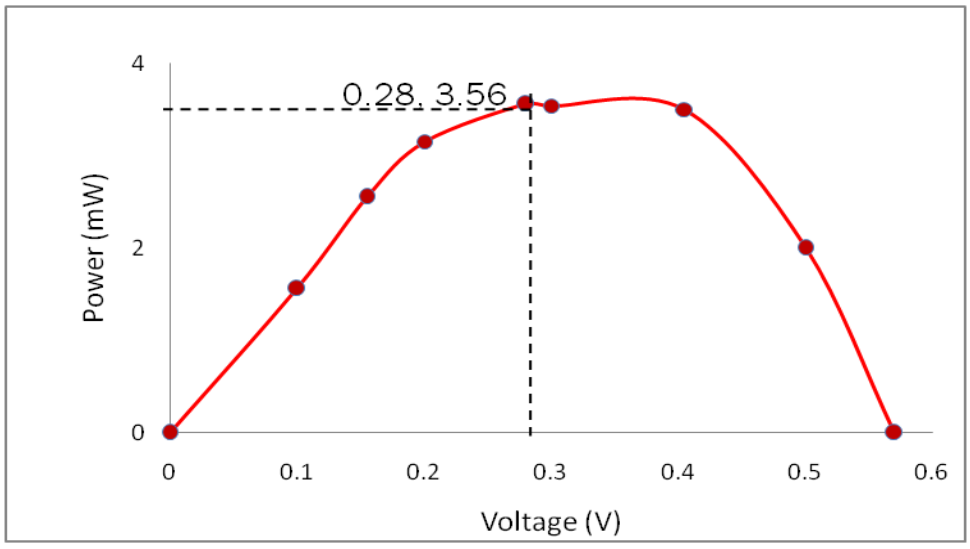
second. The instrument at first calibrated by a reference cell (mono-silicon solar cell) supplied by Gratings Inc.

Table 6.6 Data for reference cell

Parameters	Data for reference cell
V_{oc}	0.62 V
I_{sc}	28.68 mA
FF	52.95
η	14.63 %
V_{mp}	0.38 V
I_{mp}	24.512 mA
P_{max}	9.36 mW



(a)



(b)

Figure 6.12 (a) I-V curve (b) P versus V curve for mono-silicon solar cell (125×125 mm^2)

Table 6.7 Findings from in house fabricated mono-silicon solar cell (125×125 mm^2)

Parameters	Data for fabricated cell
V_{oc}	0.57 V
I_{sc}	18.144 mA
FF	37.14
η	5.96 %
V_{mp}	0.28 V
I_{mp}	13.8 mA
P_{max}	3.56 mW

6.11 Summary

SPV technique is used to determine the minority carrier diffusion length and the result is $110\,\mu m$ for in-house fabricated mono-silicon solar cell. This measurement is helped to calculate minority carrier lifetime and the result is $4.48\,\mu s$. Carrier generation, recombination, rate of carrier generation and recombination through the entire thicknesses of the cell also calculate in this chapter.

The cell fabrication on thin (180±20 μm), mono-silicon commercial wafer of 125×125 mm^2 is possible manually. That is why I-V characterization gives the cell efficiency 5.96%. It is poor enough. Optimization is needed for each step. It is one of the main root causes of the poor efficiency. This is just the initial case as number of optimization needed for each case for which ample time is needed. However, it is well proven that this kind of process works fine to make solar cells on commercial silicon wafer.

6.12 References

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Chapter VII

Conclusion

7.1 Summary

Silicon dominated PV industries use mono crystalline silicon wafers. Mono silicon wafers have lower defects compared to others. The solar cells manufactured from these wafers are used to maximize the power density in the PV module and to reduce the cost per unit energy. To reduce the fabrication cost minimization of material cost is needed. In order to reduce the material cost, recently continuous efforts have been put on multi-wire saw technology to cut thinner wafers and reduce material consumption. A wafer with 150-200 μm thickness requires an automated advanced technology handling process to increase the yield of solar cell processing. Though the automated advanced technology increases the efficiency of solar cells, but unfortunately increases significantly the process cost due to higher equipment and maintenance additional costs. In order to reduce the manufacturing cost an approach is to focus on low budgeted manual fabrication process. But most of the laboratory scale solar cells are smaller size such as $1x1cm^2$ or $2 \times 2\ cm^2$. So, it is tough enough to reflect the optimized processes onto wafer size of 4 inch to 8 inch diameter by this low budgeted manual process. That is why an intermediate steps in between lab-scale fabrication and fully automated commercial processes are exemplified in this research.

Two key research issues have been identified in this study regarding to low budgeted manual fabrication process. The first key research issue is to reducing the number of expensive and time consuming processing steps so that, the equipment cost can be reduced. In addition, the process requires fewer chemicals to reduce the environment pollution as well. The second key research issue is the use of low cost or multifunctional characterization equipments so that the properties change can easily be monitored.

From the identified key issues, three research objectives have been outlined. The first two research objectives are dedicated for fabrication issues. The third research objectives are designed to investigate the properties of fabricated solar cell

related issues. In order to achieve these objectives, both theoretical and practical approaches have been employed. A concise summary on the outlined objectives in this study is as below.

The first objective is to explore a simplified process for solar cell fabrication on commercial silicon wafer. The simplified process incorporates single step phosphorus diffusion, anti-reflection coating (ARC) and a surface passivation. P-type boron doped 180±20 μm thick mono crystalline silicon (100) substrates (known as commercial silicon wafer) were used for the fabrication. The RCA cleaning and texturing details for mono silicon sample were explained. The cleaning and texturing process also called isotropic and anisotropic etching where alkali solution was used. Texturing process needed iso2-propanol (IPA) for pyramid growth. The appropriate precaution should maintained before the use of IPA and HF solution. Diffusion had been done by $POCl_3$ solution at the temperature of 875°C. In this thermal diffusion process, $POCl_3$ served as the dopant source and the final incorporation of the oxygen gas produced SiO_2 anti-reflection coating (ARC) as well as surface passivation layer. Edge isolation was done by HF/HNO3 acid barrier paste which was carried out by screen printing. After that it was dried at 120ºC for 10 minutes by oven. An advantage of single side etching was preserving the active cell area. Metallization was done by Ferro FX53-038 Al paste (front contact) and Ferro CN33-462 Ag paste (back contact) by screen printing and dried at 120ºC for 10 minutes by oven. Co-firing was done by infrared lamp heated belt furnace with 500˚C, 600˚C and 800˚C at a belt speed of 40 IPM.

The second objective is to explore the thermal diffusion process by using dopant solutions P5O9. The procedures carried out at 875˚C. The P5O9 spin on dopant solution mainly comprises of P2O5 and dissolved SiO_2 in organic solvents. That is why the spin on dopant film was retained to served as an ARC and surface passivation layer after doping. In the first objective, the sample size was 125×125 mm^2; a large horizontal diffusion chamber was used, so that there needed a large amount of N_2 and O_2 gases to complete the whole processes. But for spin on doping, the sample size was 2.2×2.2 cm^2 so that required RTP chamber was small enough and comparatively fewer amounts of N_2 gases were used. Both 180±20 μm and 600±50 μm thick samples were prepared in this case. Both diffusion furnaces were horizontal

but the wafers were placed vertically for $POCl_3$ diffusion and horizontally for P5O9 diffusion.

The third objective is to explore the characterization after each step of device fabrication. Structural properties were found by scanning electron microscopy, stylus surface profilomerty etc. Electrical properties were found by four point probe, xenon lamp based sun simulator. Optical properties were found by optical microscopy, spectroscopic reflectometry, spectral reflectance measurement, surface photo voltage measurement. Wafers had been characterized by using a in-house made hot probe tool. Hot probe characteristic curves were taken for temperature 50˚C -80˚C. Theoretical studies on temperature dependent majority charge carrier concentration, impurity concentration and thermally generated charge carrier concentration had been conducted through equation derivation. Practical results agreed with the theoretical explanation. Wafer thickness was measured by dial indicator. Surface topography was analyzed by SEM with 1000x-20,000x magnification. 2D Optical microscopy also helped to show the surface images as well. EDS could measure the elemental presence in the sample. Dektak 150 stylus surface profilometer is a thin film thickness measurement tool. An approach of measuring the textured surface pyramid heights by Dektak 150 stylus surface profilometer was a new concept. Pyramid heights were found 2.97, 3.12 microns that was matched with the ideal value. The measurement technique was simple, easy and innovative. Sheet resistivity and physical resistivity of raw and doped silicon samples were measured by four point probe. All optical measurement performed inside dark room to avoid any additional light source. Spectroscopic reflectometer and spectral reflectance measurement could measure light reflection from the substrate surface. Result showed the remarkable reduction of light reflection from the cell surface. The SiO_2 (anti reflection coating) film thicknesses of 101 nm was achieved by spectroscopic reflectometer also. Minority carrier diffusion length $110\,\mu m$ was found by SPV technique. Calculated minority carrier lifetime was $4.48\,\mu s$. Carrier generation, recombination, rate of carrier generation and recombination through the entire thicknesses of the cell was also calculated. The cell efficiency was achieved 5.96% by I-V characterization. The result is poor enough because of the total procedure was go through manual in-hand operations with low cost instrumentations on thin commercial wafer. Optimization is needed for each step. It is one of the main root causes of the poor efficiency.

7.2 Future Recommendations

Based on the findings in this study, several potential notions on improving the performance of the quality of the device fabricated are proposed as follows:

The use of standard clean room during fabrication can improve the quality of solar cell. An ISO 9 clean room generally contains more than 30 million particles of 0.5 μm diameter (or more) per cubic meter, where as an ISO 1 clean room has almost no particles of 0.5 μm diameter per cubic meter except 2 particles of 0.2 μm and smaller. U.S. General Service Administration's standards (FS209E) class 100 to 1000 equivalents to International Standards Organization (ISO) ISO 5 – ISO 6 class requirement was not meet during the solar cell fabrication in the Laboratory. 2400 laser particle counter counts the particle that shows the clean in between ISO 7 and ISO 8. Before go through industrial manufacturing process one must focus on the standard clean room facility.

Mono-crystalline Si wafers are widely used in PV industries. Because it has lower defects and imparts (produce) the reduced cost solar cell per unit energy which is varied from 0.77 to 0.86 $. The concentration of foreign particles such as oxygen, carbon, and metallic impurity during the wafer processing is an important factor that limits the efficiency of solar cells. In that sense Fz wafer is better than Cz wafer. But Fz wafer is costly Multi-wire saw technology is recently used to cut thinner wafers and reduce material consumption and cost. A wafer with <200 μm thickness requires an automated handling process for solar cell fabrication processing. But in case of manual handling process 200 μm thickness wafers were chosen to handle carefully. However, reducing the wafer thickness affects the electrical performance of solar cells. A compromise in-between material consumption and power output is needed to address focus. Most of industrial solar cells are based on p-type wafers and n-type diffused emitter. The n-type wafers have very high τeff (411μs) and long diffusion length so that the wafers price still much higher than p-type. But power is degraded in p-type cell by *3-5* % due to minority carrier life time degradation which is a result of boron-oxygen related metastable defect under illumination. A compromise in-between p-type and n-type is needed.

In this research wafer cleaning and texturing uses reduced chemicals in order to reduce costs and environment pollution. NaOH/KOH and isopropyl alcohol (IPA)

are widely used in the standard alkaline texturization procedure where IPA promotes the formation of pyramidal structure. The key parameters for uniform texturization are the surface preparation, process temperature, solution concentration, dosing rate and evaporation rate of IPA which need to be controlled. Note that one sided mirror polished wafer is not suitable for higher wet ability and produce non-uniform pyramids. The boiling point of IPA is 82.4 °C that is why it shows higher evaporation rate. Carbohydrates can be introduced in the replacement of IPA.

Single side etching in PV industries is widely used. Single side HF/HNO3 acid barrier paste was used for edge isolation by screen printing. The major advantages of this process are, it preserves the active cell area, lower parasitic loss, higher FF compared to laser isolation. But many of the fabricated cell faced short circuit in this research. That is why laser isolation was used. But it reduces the active cell area. So, an alternate procedure of edge isolation needs to be investigated to minimize this problem.

The rapid thermal procedure for annealing requires additional care as this process applies heat to the whole sample at once which may cause degradation of material quality. Ramp of heating and hence calibration could be exercised to have a control over rapid thermal annealing. Oxygen and Nitrogen gas supply need to be ensured during this process to avoid short circuit. Better methods of handling and transferring samples from one system to another without exposure to atmosphere, by using portable desiccated and sealable chamber, need to be ensured.

The minority carrier diffusion length needs to be in the range of 100-300 μm. The findings were 110 μm which was much lower. Measurement of minority carrier life time was much below than 10 μsec. It can be ameliorated if the above processes are amended.

The front contact contains two bus bars. It can be replaced by three bus bars that will increase the carrier collection efficiency. For characterization of complete cells proper probing is important issue. Additional silver coating need to be used on the aluminum coated back side.

Series and shunt resistance gives the information of the quality of solar cells. The LIV tester did not provide those information while measuring efficiencies. It needs to be measured in future.

In future, the significant enhancement could be made for the hot probe experiment by conducting the experiment in vacuum. Another point is thermally conducting paste could be used between the contacts to improve the thermal conduction. Doping uniformity has been checked by this hot probe instrument. Alternate procedure is to be investigated for better understanding.

Optimization is needed for each step. It is one of the main root causes of the poor efficiency. This is just the initial case as number of optimization needed for each case for which extensive time is needed. However, it is well proven that this kind of process works fine to make solar cells on commercial silicon wafer.

Appendix I

Fabrication tool

In this section we have presented the images of several fabrication tools those were used in the fabrication of silicon solar cell.

A. DI water plant for sample preparation

The de-ionized water plant from Siemens used to produce ultra pure De-ionized water. This water purification unit is established in the Centre of Excellence for VLSI Technology, Institute of Electronics, Atomic Energy Research Establishment, Savar, Dhaka.

The systems use ion exchange membranes and ion exchange resins to produce consistent high-quality water with no regeneration. Almost 99.5% salt removed from the product water and its resistivity is 18.2 MΩ-cm (conductivity is 0.055 micromho/cm) [1,2].

Figure App 1: Front side view of De-ionized water plant.

B. Laser Cutter

The laser cutting machine was used in our study to cut solar cell is supplied from YUEMAO YMS-50D, China. The instrument is established in the Advanced Solar Cell Fabrication Laboratory, Solar Energy Research Institute (SERI), Universiti Kebangsaan, Malaysia (UKM).

It has excellent beam quality, system reliability, friendly man-machine interface with a simple software operation [3,4].

Figure App 2: (a) Front side view of laser cutter (b) Silicon wafer under the laser cutter

C. Fume hood for avoid inhaling toxic gases

The general type fume hood was used as work bench for cleaning and etching of silicon wafer. The instrument established in thin Film Laboratory, Solar Energy Research Institute, Universiti Kebangsaan, Malaysia. This type of fume hood represents it as a local ventilation device that is designed to limit exposure to hazardous gas or toxic fumes, vapours or dusts [5].

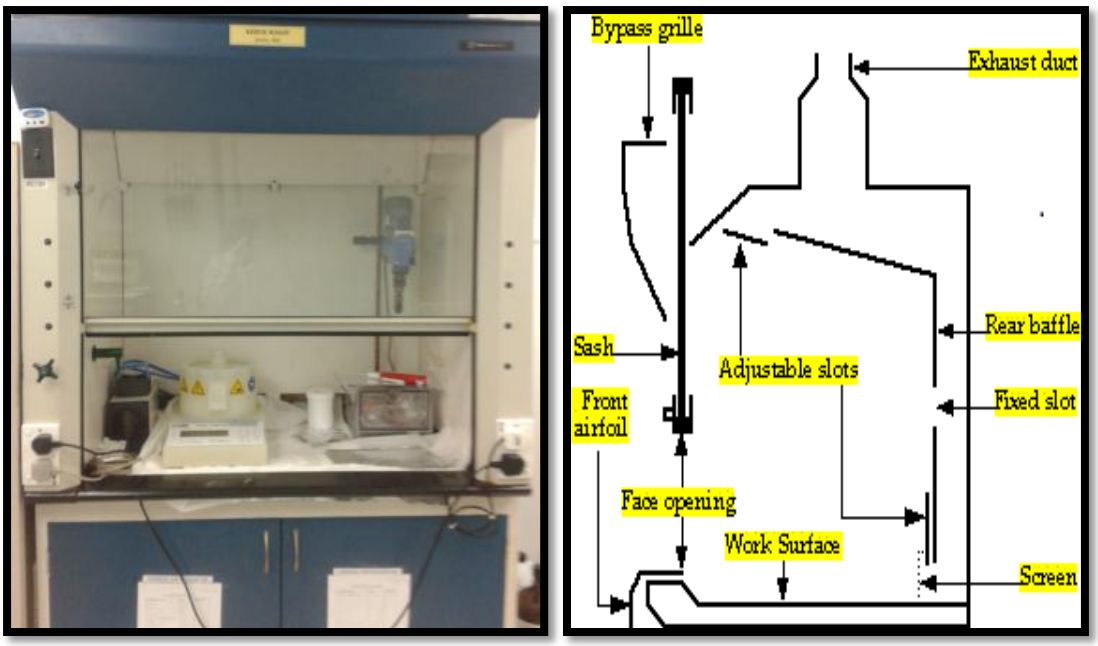


Figure App 3: (a) Front side view of fume hood (b) Basic parts of fume hood

D. Sample cleaning bath

The three chambers of cleaning bath was used for chemical cleaning and etching of samples. This unit is established in the Solar Cell Fabrication Laboratory, Institute of Electronics, Atomic Energy Research Establishment, Savar, Dhaka.

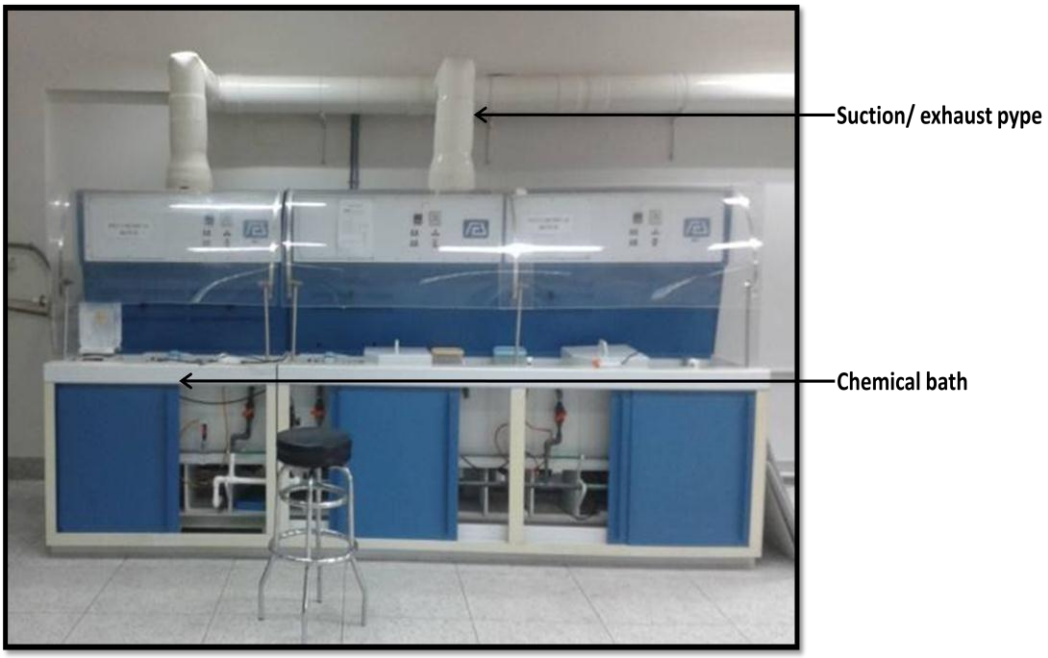


Figure App 4: Front side view of sample cleaning bath

E. Hot Plate

The hot plate from Fisher Scientific™ Isotemp™ with Ceramic Tops is established in Thin Film Laboratory, Solar Energy Research Institute (SERI), Universiti Kebangsaan Malaysia (UKM). Its controller type is analog with LED display. Its safety warning system with visual alert protects user from accidental burns. It has also redundant temperature control systems for over temperature protection [6,7].

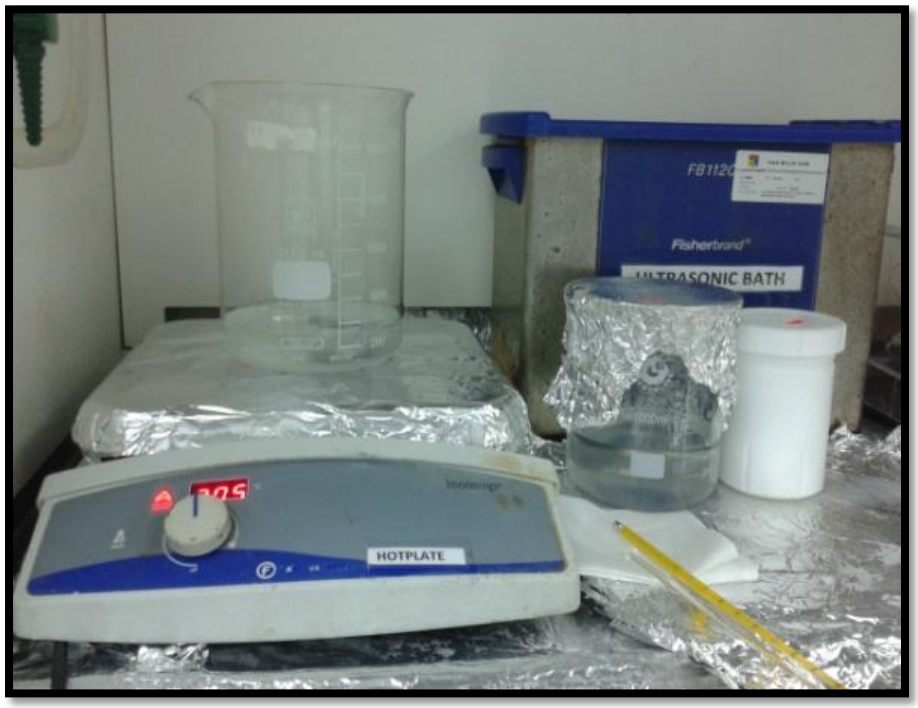


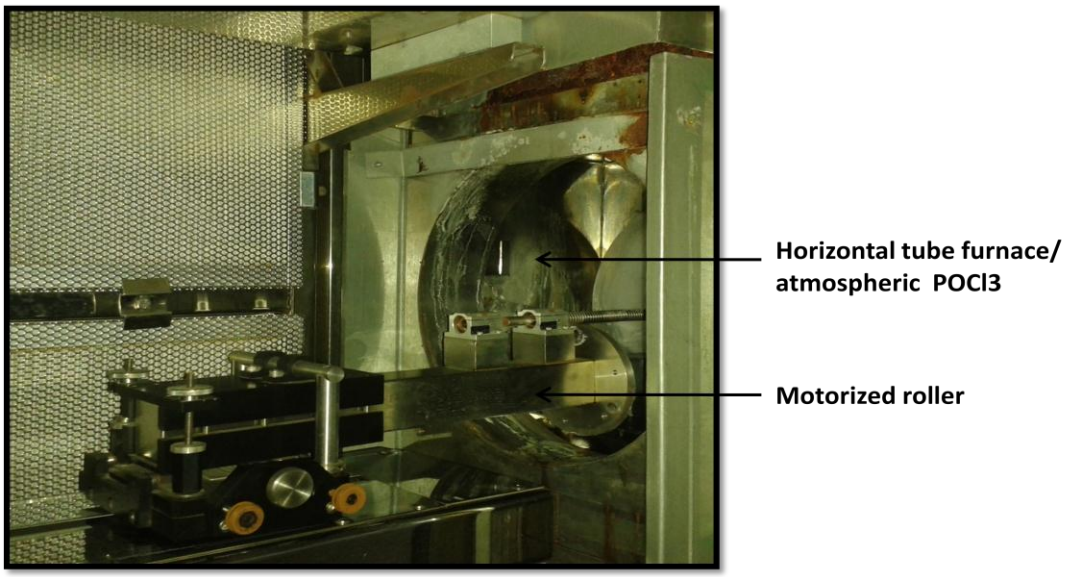
Figure App 5: Front side view of hot plate

F. Diffusion furnace

The horizontal tube heating furnace from Sandvik's MRL phoenix used to diffuse phosphorus into the silicon wafer. This furnace is established in Solar Cell Fabrication Laboratory, Institute of Electronics, Atomic Energy Research Establishment, Savar, Dhaka.

This instrument covers an extensive range of temperatures for solar cell processing. It has three tubes, 40"-48" thermal flat zone and compatible for 100 -300 mm substrate. Its temperature uniformity is excellent [8,9].

(a)



(b)

Figure App 6: (a) Front side view of diffusion furnace (b) Motorized channel carry the wafer inside the horizontal diffusion furnace

G. Spin Coater

The spin coater from SPS Spin 150 spin coater is used to produce a thin layer of dopant solution on the silicon sample. This spin coater is established in Thin Film Laboratory, Solar Energy Research Institute (SERI), Universiti Kebangsaan Malaysia (UKM).

Two step programming had done by this device for the spin on dopant solution P5O9 . The coater offers a vacuum secured sample holder with capabilities ranging from very small samples to up to 150 mm diameter or 101.6 mm x 101.6 mm square substrates. The programs were easy to set up with up to 99 steps per program, 0 - 2,000 rpm/sec^2 acceleration, a max speed of 10,000 rpm and a maximum time per step of 6000 seconds [10,11,12].

Figure App 7: Front side view of spin coater

H. Annealing Furnace

The rapid thermal processing tube furnace from MTI Corporation OTF-1200 X is used to annealing silicon wafers for solar cell fabrication. This annealing furnace is established in Thin Film Laboratory, Solar Energy Research Institute (SERI), Universiti Kebangsaan Malaysia (UKM).

This instrument has 4" quartz tube and vacuum flanges and its halogen light tube is used as the heating element for 12" length with 4" constant temperature zone within +/-5 □C uniformity. K type thermocouple is used and 30 programmable segments used for precise control of heating rate, cooling rate and dwell time. EQ-FYP vacuum pump is recommended for this furnace [13,14].

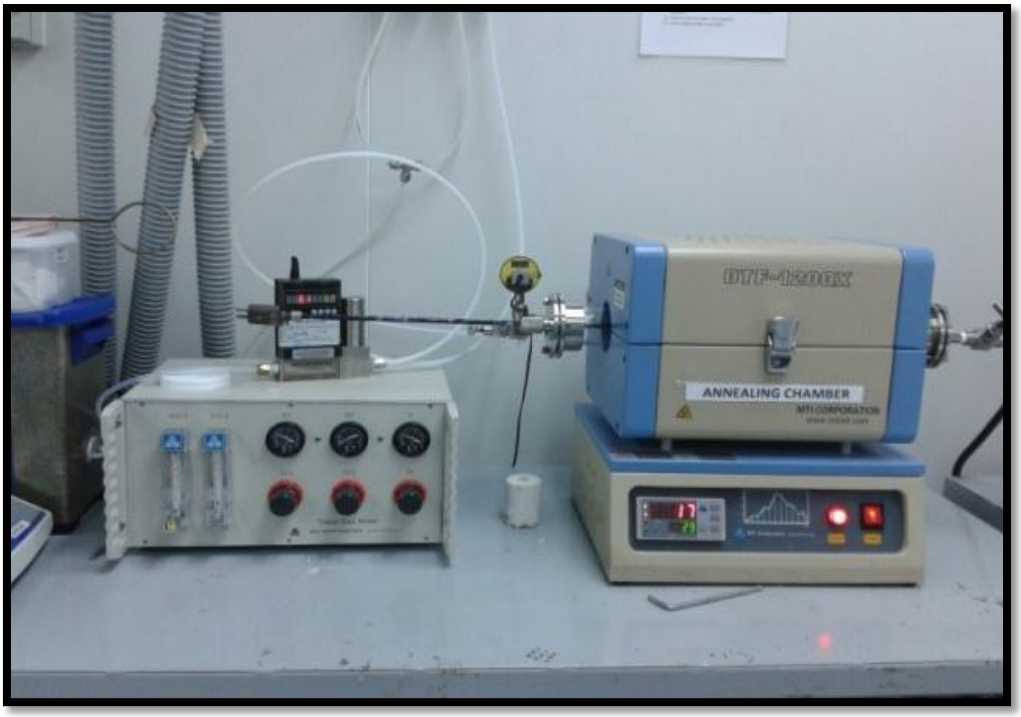


Figure App 8: Front side view of annealing furnace

I. Screen Printer

The screen printer is used for contact printing and is established in Solar Cell Fabrication Laboratory, Institute of Electronics, Atomic Energy Research Establishment, Savar, Dhaka.

Figure App 9: Screen printer

J. RTA Belt Furnace

The conveyor belt furnace of RTC MODEL RF-306 is used to carry the solar cells through the primary heating chamber for rapid thermal processing. The furnace is established in Solar Cell Fabrication Laboratory, Institute of Electronics, Atomic Energy Research Establishment, Savar, Dhaka.

The instrument is composed of multiple controlled zones which includes preheating zone, binder burn out zone, heating zone, firing zone and cooling zone. The firing is done at a temperature of about 700-800 °C for about one minute. Upon firing, the organic solvents evaporate and the metal paste becomes a conducting path for the electric current [15, 16].

Figure App 10: Front side view of RTA belt furnace

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Appendix II

Spectral Reflectance Measurement (SRM) data

Wavelength (λ) nm	Mirror (AU)	Raw (AU)	% raw	Cleaned (AU)	% cleaned	Textured (AU)	% textured
450	0.087673	0.019288	22.01	0.027854	31.77	0.013151	15.001
500	0.292401	0.052632	18.01	0.079094	27.05	0.035088	12.01
550	0.80426	0.113964	14.17	0.189805	23.6	0.07737	9.62
600	1.640238	0.230289	14.04	0.361672	22.05	0.154355	9.41052
650	2.708453	0.366183	13.52	0.570129	21.05	0.247739	9.1469
700	4.640623	0.591215	12.74	0.968869	20.878	0.38519	8.3004
750	5.488286	0.680987	12.408	1.113299	20.285	0.455528	8.30
800	5.648857	0.704243	12.467	1.139374	20.17	0.451909	8.001
850	6.098089	0.760188	12.466	1.201567	19.704	0.426866	7.10
900	7.853732	0.785373	10.001	1.461312	18.6066	0.534054	6.80
950	9.394891	0.751591	8.1	1.643166	17.49	0.544904	5.80
1000	9.768766	0.683814	7.01	1.661472	17.008	0.488438	5.001

Appendix III

Surface photovoltage versus wavelength data

Wavelength (λ)	Surface photovoltage (AU)
700	0.549351
720	0.803373
740	1.457768
760	2.558971
780	2.810093
800	2.931317
820	3.591509
840	3.177514
860	1.918306
880	1.599636
900	0.856361
920	1.129655
940	0.997974
960	0.541249
980	0.641468
1000	0.640592

1/Vspv versus 1/alpha data

Wavelength (λ)	alpha/cm	1/alpha in micrometer	1/Vspv
700	1.90E+03	5.263157895	1.820329807
720	1.66E+03	6.024096386	1.244751815
740	1.42E+03	7.042253521	0.685980211
760	1.19E+03	8.403361345	0.390782076
780	1.01E+03	9.900990099	0.355860109
800	8.50E+02	11.76470588	0.341143588
820	7.07E+02	14.14427157	0.278434496
840	5.91E+02	16.92047377	0.314711438
860	4.80E+02	20.83333333	0.521293266
880	3.83E+02	26.10966057	0.62514222
900	3.06E+02	32.67973856	1.167731833

920	2.40E+02	41.66666667	0.88522602
940	1.83E+02	54.64480874	1.002030113
960	1.34E+02	74.62686567	1.847578471
980	9.59E+01	104.2752868	1.558924218
1000	6.40E+01	156.25	1.561056023

Carrier Generation

Thickness (μm)	G (tot) (/cm^{2}s)	G 37% in emitter	G 14% in junction	G 49% in base
0	1.13E+21	4.181E+20	1.582E+20	5.537E+20
5	2.26512E+19	8.38094E+18	3.17117E+18	1.10991E+19
10	1.13256E+19	4.19047E+18	1.58558E+18	5.54954E+18
15	7.5504E+18	2.79365E+18	1.05706E+18	3.69969E+18
20	5.6628E+18	2.09523E+18	7.92792E+17	2.77477E+18
25	4.53024E+18	1.67619E+18	6.34233E+17	2.21982E+18
30	3.7752E+18	1.39682E+18	5.28528E+17	1.84985E+18
35	3.23588E+18	1.19728E+18	4.53024E+17	1.58558E+18
40	2.8314E+18	1.04762E+18	3.96396E+17	1.38739E+18
45	2.5168E+18	9.31215E+17	3.52352E+17	1.23323E+18
50	2.26512E+18	8.38094E+17	3.17117E+17	1.10991E+18
55	2.0592E+18	7.61904E+17	2.88288E+17	1.00901E+18
60	1.8876E+18	6.98412E+17	2.64264E+17	9.24923E+17
65	1.7424E+18	6.44688E+17	2.43936E+17	8.53775E+17
70	1.61794E+18	5.98638E+17	2.26512E+17	7.92792E+17
75	1.51008E+18	5.58729E+17	2.11411E+17	7.39939E+17
80	1.4157E+18	5.23809E+17	1.98198E+17	6.93693E+17
85	1.33242E+18	4.92996E+17	1.86539E+17	6.52887E+17
90	1.2584E+18	4.65608E+17	1.76176E+17	6.16616E+17
95	1.19217E+18	4.41102E+17	1.66903E+17	5.84162E+17
100	1.13256E+18	4.19047E+17	1.58558E+17	5.54954E+17
105	1.07863E+18	3.99092E+17	1.51008E+17	5.28528E+17
110	1.0296E+18	3.80952E+17	1.44144E+17	5.04504E+17
115	9.84834E+17	3.64389E+17	1.37877E+17	4.82569E+17
120	9.43799E+17	3.49206E+17	1.32132E+17	4.62462E+17
125	9.06047E+17	3.35238E+17	1.26847E+17	4.43963E+17
130	8.71199E+17	3.22344E+17	1.21968E+17	4.26888E+17
135	8.38933E+17	3.10405E+17	1.17451E+17	4.11077E+17
140	8.08971E+17	2.99319E+17	1.13256E+17	3.96396E+17
145	7.81075E+17	2.88998E+17	1.09351E+17	3.82727E+17
150	7.5504E+17	2.79365E+17	1.05706E+17	3.69969E+17

155	7.30683E+17	2.70353E+17	1.02296E+17	3.58035E+17
160	7.0785E+17	2.61904E+17	9.90989E+16	3.46846E+17
165	6.864E+17	2.53968E+17	9.60959E+16	3.36336E+17
170	6.66211E+17	2.46498E+17	9.32696E+16	3.26444E+17
175	6.47177E+17	2.39455E+17	9.06047E+16	3.17117E+17
180	6.292E+17	2.32804E+17	8.80879E+16	3.08308E+17
185	6.12194E+17	2.26512E+17	8.57072E+16	2.99975E+17
190	5.96084E+17	2.20551E+17	8.34517E+16	2.92081E+17
195	5.808E+17	2.14896E+17	8.13119E+16	2.84592E+17
200	5.6628E+17	2.09523E+17	7.92792E+16	2.77477E+17

Carrier Recombination

Thickness (μm)	R (tot) (/cm^{2}s)	R in emitter 75%	R in junction 2%	R in base 23%
0	4.4409E+20	3.13575E+20	3.164E+18	1.27351E+20
5	8.90192E+18	6.2857E+18	6.34233E+16	2.55279E+18
10	4.45096E+18	3.14285E+18	3.17117E+16	1.27639E+18
15	2.96731E+18	2.09523E+18	2.11411E+16	8.5093E+17
20	2.22548E+18	1.57143E+18	1.58558E+16	6.38197E+17
25	1.78038E+18	1.25714E+18	1.26847E+16	5.10558E+17
30	1.48365E+18	1.04762E+18	1.05706E+16	4.25465E+17
35	1.2717E+18	8.97958E+17	9.06047E+15	3.64684E+17
40	1.11274E+18	7.85713E+17	7.92792E+15	3.19099E+17
45	9.89102E+17	6.98412E+17	7.04704E+15	2.83643E+17
50	8.90192E+17	6.2857E+17	6.34233E+15	2.55279E+17
55	8.09265E+17	5.71428E+17	5.76576E+15	2.32072E+17
60	7.41826E+17	5.23809E+17	5.28528E+15	2.12732E+17
65	6.84763E+17	4.83516E+17	4.87872E+15	1.96368E+17
70	6.35851E+17	4.48979E+17	4.53024E+15	1.82342E+17
75	5.93461E+17	4.19047E+17	4.22822E+15	1.70186E+17
80	5.5637E+17	3.92857E+17	3.96396E+15	1.59549E+17
85	5.23642E+17	3.69747E+17	3.73078E+15	1.50164E+17
90	4.94551E+17	3.49206E+17	3.52352E+15	1.41822E+17
95	4.68522E+17	3.30827E+17	3.33807E+15	1.34357E+17
100	4.45096E+17	3.14285E+17	3.17117E+15	1.27639E+17
105	4.23901E+17	2.99319E+17	3.02016E+15	1.21561E+17
110	4.04633E+17	2.85714E+17	2.88288E+15	1.16036E+17
115	3.8704E+17	2.73291E+17	2.75754E+15	1.10991E+17
120	3.70913E+17	2.61904E+17	2.64264E+15	1.06366E+17
125	3.56077E+17	2.51428E+17	2.53693E+15	1.02112E+17

130	3.42381E+17	2.41758E+17	2.43936E+15	9.81842E+16
135	3.29701E+17	2.32804E+17	2.34901E+15	9.45477E+16
140	3.17926E+17	2.24489E+17	2.26512E+15	9.1171E+16
145	3.06963E+17	2.16748E+17	2.18701E+15	8.80272E+16
150	2.96731E+17	2.09523E+17	2.11411E+15	8.5093E+16
155	2.87159E+17	2.02765E+17	2.04591E+15	8.2348E+16
160	2.78185E+17	1.96428E+17	1.98198E+15	7.97746E+16
165	2.69755E+17	1.90476E+17	1.92192E+15	7.73572E+16
170	2.61821E+17	1.84874E+17	1.86539E+15	7.5082E+16
175	2.5434E+17	1.79592E+17	1.81209E+15	7.29368E+16
180	2.47275E+17	1.74603E+17	1.76176E+15	7.09108E+16
185	2.40592E+17	1.69884E+17	1.71414E+15	6.89943E+16
190	2.34261E+17	1.65413E+17	1.66903E+15	6.71786E+16
195	2.28254E+17	1.61172E+17	1.62624E+15	6.54561E+16
200	2.22548E+17	1.57143E+17	1.58558E+15	6.38197E+16

Carrier generation rate

Thickness (μm)	generation rate(/cm^{3}s)
0	1.48294E+20
5	2.9726E+18
10	1.4863E+18
15	9.90866E+17
20	7.43149E+17
25	5.94519E+17
30	4.95433E+17
35	4.24657E+17
40	3.71575E+17
45	3.30289E+17
50	2.9726E+17
55	2.70236E+17
60	2.47716E+17
65	2.28661E+17
70	2.12328E+17
75	1.98173E+17
80	1.85787E+17
85	1.74859E+17
90	1.65144E+17
95	1.56452E+17
100	1.4863E+17

105	1.41552E+17
110	1.35118E+17
115	1.29243E+17
120	1.23858E+17
125	1.18904E+17
130	1.14331E+17
135	1.10096E+17
140	1.06164E+17
145	1.02503E+17
150	9.90866E+16
155	9.58902E+16
160	9.28936E+16
165	9.00787E+16
170	8.74293E+16
175	8.49313E+16
180	8.25721E+16
185	8.03404E+16
190	7.82262E+16
195	7.62204E+16
200	7.43149E+16

Carrier recombination rate

Thickness (μm)	recom rate (/cm^{3}s)
0	5.82795E+19
5	1.16823E+18
10	5.84115E+17
15	3.8941E+17
20	2.92058E+17
25	2.33646E+17
30	1.94705E+17
35	1.6689E+17
40	1.46029E+17
45	1.29803E+17
50	1.16823E+17
55	1.06203E+17
60	9.73525E+16
65	8.98639E+16
70	8.3445E+16
75	7.7882E+16
80	7.30144E+16

85	6.87194E+16
90	6.49017E+16
95	6.14858E+16
100	5.84115E+16
105	5.563E+16
110	5.31014E+16
115	5.07926E+16
120	4.86763E+16
125	4.67292E+16
130	4.49319E+16
135	4.32678E+16
140	4.17225E+16
145	4.02838E+16
150	3.8941E+16
155	3.76849E+16
160	3.65072E+16
165	3.54009E+16
170	3.43597E+16
175	3.3378E+16
180	3.24508E+16
185	3.15738E+16
190	3.07429E+16
195	2.99546E+16
200	2.92058E+16