Experimental Study on the Effect of different etching methods for texturization of mono-cSI wafers required for the fabrication of solar cells

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DECLARATION OF ORIGINAL WORK

Supervisor's Declaration

The MS level research titled by "**Experimental Study on the Effect of different etching methods for texturization of mono-cSI wafers required for the fabrication of solar cells"** has been carried out and the dissertation was prepared under my direct supervision. Hereby I confirm that, to the best of my knowledge the thesis represents the original research work of the candidate; the contribution made to the research by me, by others of the University was consistent with normal supervisory practice, and external contributions to the research are acknowledged.

I believe the thesis to be in a suitable presentational form and ready for examination.

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Candidate's Declaration

I confirm that this thesis represents my own work; the contribution of any supervisors and others to the research and to the thesis was consistent with normal supervisory practice. External contributions to the research are acknowledged.

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Abstract: Etching methods were developed for texturization study on mono-cSi wafer required to have a fabrication processing of solar cells. The etching effects on quantum efficiency of solar cells. We compare three different etching methods (Recipe 1: CH_4O/ C_3H_6O, recipe 2: NaOH/HF, Recipe 3: HNO_3/HF) on surface texturization of mono-crystalline Si wafers in an KOH/IPA solution. With a better saw damage removal method bigger pyramids can be seen than those at the more contaminated zones, causing homogenous textured figure and reflectance uniformity on wafer surfaces. Spectral response measurement system (200mv/ 400nm-1200nm) and Scanning electron microscope (operated at 20 KV, magnification: ×5000- ×50000) were used to differentiate the etching quality of several recipes by analyzing change of reflectance and surface morphology respectively. Bigger pyramids found on mono-cSI wafer etching by method 1, which reflects the quality of reflectance of wafer. Spectral response of this wafer was also studied. Percentage Reflectance with respect to mirror image was measured from graphical analysis. Saw damage removal process may require to be customized to attain consistent and desired texturization outputs.

Chapter 1

Introduction

1.1. World's energy Consumption and resources

World energy consumption refers to the total energy used by all of human civilization. Typically measured per year, it involves all energy harnessed from every energy source applied towards humanity's endeavors across every single industrial and technological sector, across every country. Being the power source metric of civilization. World Energy Consumption has deep implications for humanity's social-economic-political sphere. (1)

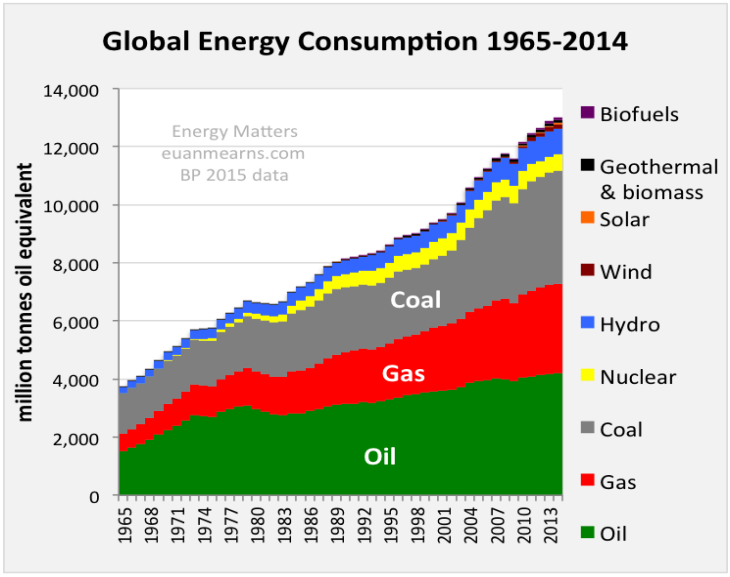


Figure1.1: Global energy consumption

The world's energy resources can be divided into fossil fuel, nuclear fuel and renewable resources. The estimation for the amount of energy in these resources is given in zeta joules (ZJ), which is 10^{21} joules. (2)

Fossil fuel

Remaining reserves of fossil fuel are estimated as: coal, oil and gas 19.8Zj, 8.1Zj and 8.1Zj respectively (proven energy reserves at the end of 2009). Rreserves may be up to a factor 4 larger. Significant uncertainty exists for these numbers. Estimating the remaining fossil fuels on the planet depends on a detailed understanding of the Earth's crust. While modern drilling technology makes it possible to drill wells in up to 3 km of water to verify the exact composition of the geology, one half of the ocean is deeper

than 3 km, leaving about a third of the planet beyond the reach of detailed analysis.

In addition to uncertainty in real reserves, there is significant uncertainty in technological and economical factors that impact what percentage of reserves can be recovered gainfully. In general the easiest to reach deposits are the first extracted. Factors affecting the cost of exploiting the remaining reserves include the accessibility of fossil deposits, the level of sulfur and other pollutants in the oil and the coal, transportation costs, and societal instability in producing regions.

Nuclear energy

The International Atomic Energy Agency estimates the remaining uranium resources to be equal to 2500 ZJ. This assumes the use of breeder reactors, which are able to create more fissile material than they consume. IPCC estimated currently proved economically recoverable uranium deposits for once-through fuel cycles reactors to be only 2 ZJ. The ultimately recoverable uranium is estimated to be 17 ZJ for once-through reactors and 1000 ZJ with reprocessing and fast breeder reactors.

Resources and technology do not constrain the capacity of nuclear power to contribute to meeting the energy demand for the 21st century. However, political and environmental concerns about nuclear safety and radioactive waste started to limit the growth of this energy supply at the end of last century, particularly due to a number of nuclear accidents.

Although at the beginning of the 21st century uranium is the primary nuclear fuel world-wide, others such as thorium and hydrogen had been under investigation since the middle of the 20th century.

Thorium reserves significantly exceed those of uranium, and of course hydrogen is abundant. It is also considered by many to be easier to obtain than uranium. While uranium mines are enclosed underground and thus very dangerous for the miners, thorium is taken from open pits, and is estimated to be roughly three times as abundant as uranium in the Earth's crust.

Since the 1960s, numerous facilities throughout the world have burned Thorium.

Alternatives for energy production through fusion of hydrogen have been under investigation since the 1950s. No materials can withstand the temperatures required to ignite the fuel, so it must be confined by methods which use no materials. Magnetic and inertial confinement are the main alternatives both of which are hot research topics in the early years of the 21st century.

Renewable Energy

Renewable resources are available each year, unlike non-renewable resources, which are eventually depleted. A simple comparison is a coal mine and a forest. While the forest could be depleted, if it is managed it represents a continuous supply of energy, vs. the coal mine, which once has been exhausted is gone. Most of earth's available energy resources are renewable resources. Renewable resources account

for more than 93 percent of total U.S. energy reserves. Annual renewable resources were multiplied times thirty years for comparison with non-renewable resources. In other words, if all non-renewable resources were uniformly exhausted in 30 years, they would only account for 7 percent of available resources each year, if all available renewable resources were developed.

1.2. Renewable energy in Bangladesh (3)

Renewable energy in Bangladesh refers to the use of renewable energy to generate electricity in Bangladesh. The current renewable energy comes from biogas, hydro power, solar and wind.

Solar power

The long term average sunshine data indicates that the period of bright sunshine hours in the coastal regions of Bangladesh varies from 3 to 11 hours daily. The insolation in Bangladesh varies from 3.8 kwh/m^2/day to 6.4 kwh/m^2/day at an average of 5 kwh/m^2/day. These indicate that there are good prospects for solar thermal and photovoltaic application in the country.

With an estimated 40% of the population in Bangladesh having no access to electricity, the government introduced a scheme known as solar home systems (SHS) to provide electricity to households with no grid access.The program reached 3 million households as of late 2014 and, with more than 50,000 systems being added per month since 2009, the World Bank has called it "the fastest growing solar home system program in the world."

The Bangladeshi government is working towards universal electricity access by 2021 with the SHS program projected to cover 6 million households by 2017.

Wind Power

The long term wind flow, especially in the islands and the southern coastal belt of Bangladesh indicate that the average wind speed remains between 3 to 4.5 m/s for the months of March to September and 1.7 to 2.3 for remaining period of the year. There is a good opportunity in island and coastal areas for the application of wind mills for pumping and electrification. But during the summer and monsoon seasons (March to October) there can be very low pressure areas and storm wind speeds 200 to 300 kmph can be expected. Wind turbines have to be strong enough to withstand these high wind speeds.

Tidal Power

The tides at Chittagong Division are predominantly semidiurnal with a large variation in range corresponding to the seasons, the maximum occurring during the south-west monsoon. In 1984, an attempt was made by the Electronics and electrical engineering department of BUET to assess the feasibility of tidal energy in the coastal regions of Bangladesh, especially at Cox's Bazar and at the islands of Maheshkhali and Kutubdia. The average tidal range was found within 4-5 meter and the amplitude of the spring tide exceeds even 6 meter.[10] From different calculations, it is anticipated that there are a

number of suitable sites at Cox's Bazar, Maheshkhali, Kutubdia and other places where permanent basins with pumping arrangements might be constructed which would be a double operation scheme.

Wave Energy

Bangladesh has favorable conditions for wave energy especially during the period beginning from late March to early October. Waves generated in Bay of Bengal and a result of the southwestern wind is significant. Maximum wave height of over 2 meter with an absolute maximum of 2.4 meter was recorded. The wave periods varied from 3 to 4 seconds for waves of about 0.5 meter and about 6 seconds for waves of about 2 meter.

Waste to electricity

In order to save the large cities from environment pollution, the waste management as well as electricity generation from the solid wastes program is being taken by the government.

Biogas

There mainly two types of biogas plants used in Bangladesh, floating dome typea and fixed dome type. Bag type plants are also used in the country but rarely.

1.3. Hystory of solar photovoltaic (4)

The photovoltaic effect was experimentally demonstrated first by French physicist Edmond Becquerel. In 1839, at age 19, he built the world's first photovoltaic cell in his father's laboratory. Willoughby Smith first described the "Effect of Light on Selenium during the passage of an Electric Current" in a 20 February 1873 issue of Nature. In 1883 Charles Fritts built the first solid state photovoltaic cell by coating the semiconductor selenium with a thin layer of gold to form the junctions; the device was only around 1% efficient.In 1888 Russian physicist Aleksandr Stoletov built the first cell based on the outer photoelectric effect discovered by Heinrich Hertzin 1887. In 1905 Albert Einstein proposed a new quantum theory of light and explained the photoelectric effect in a landmark paper, for which he received the Nobel Prize in Physics in 1921. Vadim Lashkaryov discovered *p*-*n*-junctions in Cu_2O and silver sulphide photocells in 1941. Russell Ohl patented the modern junction semiconductor solar cell in 1946,while working on the series of advances that would lead to the transistor. The first practical photovoltaic cell was publicly demonstrated on 25 April 1954 at Bell Laboratories. The inventors were Daryl Chapin, Calvin Souther Fuller and Gerald Pearson. Solar cells gained prominence with their incorporation onto the 1958 Vanguard I satellite. Improvements were gradual over the next two decades. However, this success was also the reason that costs remained high, because space users were willing to pay for the best possible cells, leaving no reason to invest in lower-cost, less-efficient solutions. The price was determined largely by the semiconductor industry; their move to integrated circuits in the 1960s led to the larger availability at lower relative prices. As their price fell, the price of the resulting cells did as well. These effects lowered 1971 cell costs to some $100 per watt.

Solar cells can be classified into first, second and third generation cells. The first generation cells—also called conventional, traditional or wafer-based cells—are made of crystalline silicon, the commercially

predominant PV technology, that includes materials such as polysilicon and monocrystalline silicon. Second generation cells are thin film solar cells, that include amorphous silicon, CdTe and CIGS cells and are commercially significant in utility-scale photovoltaic power stations, building integrated photovoltaics or in small stand-alone power system. The third generation of solar cells includes a number of thin-film technologies often described as emerging photovoltaics most of them have not yet been commercially applied and are still in the research or development phase. Many use organic materials, often organometallic compounds as well as inorganic substances. Despite the fact that their efficiencies had been low and the stability of the absorber material was often too short for commercial applications, there is a lot of research invested into these technologies as they promise to achieve the goal of producing low-cost, high-efficiency solar cells.

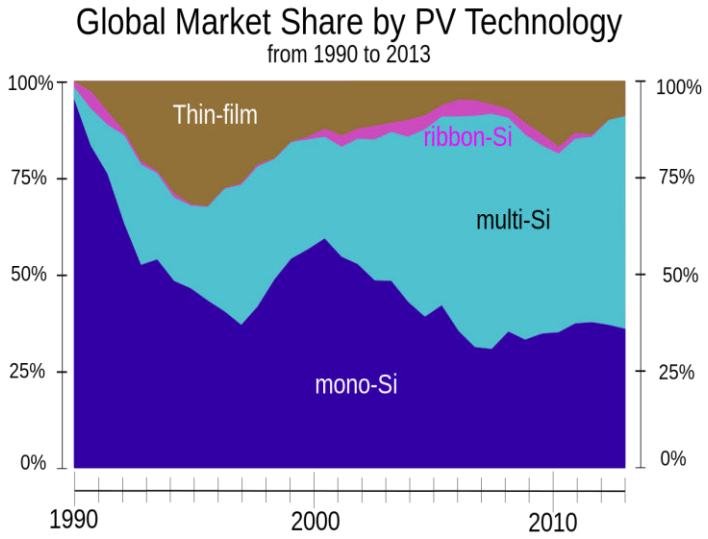


Figure1.2.: Global market share by PV technology

1.4. Application of solar cells

Cells, modules, panels and systems

Multiple solar cells in an integrated group, all oriented in one plane, constitute a solar photovoltaic panel or solar photovoltaic module. Photovoltaic modules often have a sheet of glass on the sun-facing side, allowing light to pass while protecting the semiconductor wafers. Solar cells are usually connected in series in modules, creating an additive voltage. Connecting cells in parallel yields a higher current; however, problems such as shadow effects can shut down the weaker (less illuminated) parallel string (a number of series connected cells) causing substantial power loss and possible damage because of the reverse bias applied to the shadowed cells by their illuminated partners. Strings of series cells are usually handled independently and not connected in parallel, though (as of 2014) individual power boxes are often

supplied for each module, and are connected in parallel. Although modules can be interconnected to create an array with the desired peak DC voltage and loading current capacity, using independent MPPTs (maximum power point trackers) is preferable. Otherwise, shunt diodes can reduce shadowing power loss in arrays with series/parallel connected cells.

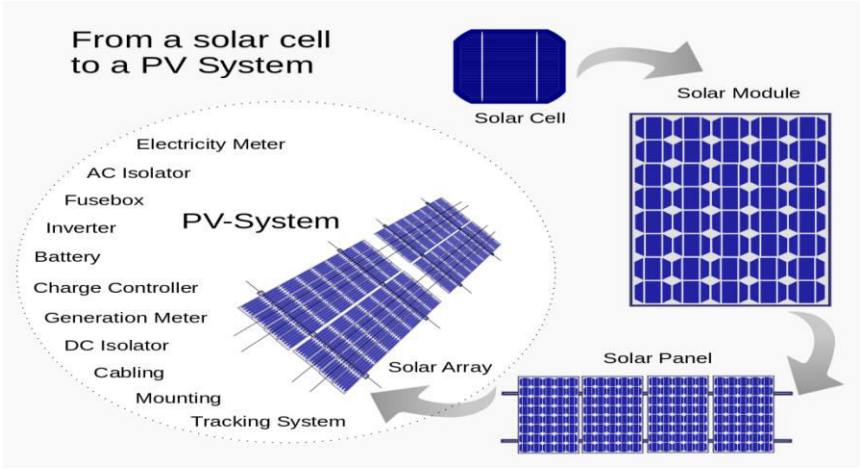


Figure 1.3: Applications of Solar cells

1.5. Arrangement of this Thesis

Chapter 2: Basic Semiconductor Properties and Physics: This chapter is about Semiconductor properties and its application in solar cells. Also, all the properties and parameters of solar cell are briefly discussed.

Chapter 3: Monocrystalline Solar Cell Fabrication: In this Chapter standard fabrication process of monocrystalline silicon solar cell have been discussed in details and explain how p-n junction is formed from p-type wafer. Also explain the requirements of preparing solar cell that can produce more electricity.

Chapter 4: Monocrystalline Solar Cell Characterization: All the techniques of optical characterization of monocrystalline solar cell is described in details. How this characterization helps to analysis the cell performance hence helps to increase the quality of a solar cell has been described in this chapter.

Chapter 5: Experimental Process and Result Analysis: Different etching method for cleaning the raw Si wafers is described. Texturing process of etched Si wafer is also described. And after texturing surface reflection measurement and scanning electron microscope image are presented with analysis.

Chapter 6: Conclusion, discuss about the result and limitation and future scope.

Chapter 2

Silicon material for photovoltaic

2.1. Introduction

Silicon is a semiconductor material which is the second most abundant element (Clarke number ~26%) on Earth and exists mainly in the oxidized silicate (SiO2) form. Si sources are neither localized in very specific regions nor are they noble. However, crystallinesilicons (c-Si) and amorphous (a-Si) silicons remain the most fundamental, purely inorganic materials used for microelectronics, optoelectronics, photonics and solar cells.

silicon is a group IV element in the periodic table of elements. This means that it has four electrons in its outermost shell, i.e., it has four valence electrons, which determines its electrical properties. Another common semiconductor is germanium that is also a group IV element. Compounds of elements for instance from groups III and V (gallium and arsenic), II and VI (cadmium and tellurium) and even I, III and VI (copper, indium and selenide) are also used to produce semiconductors (5).

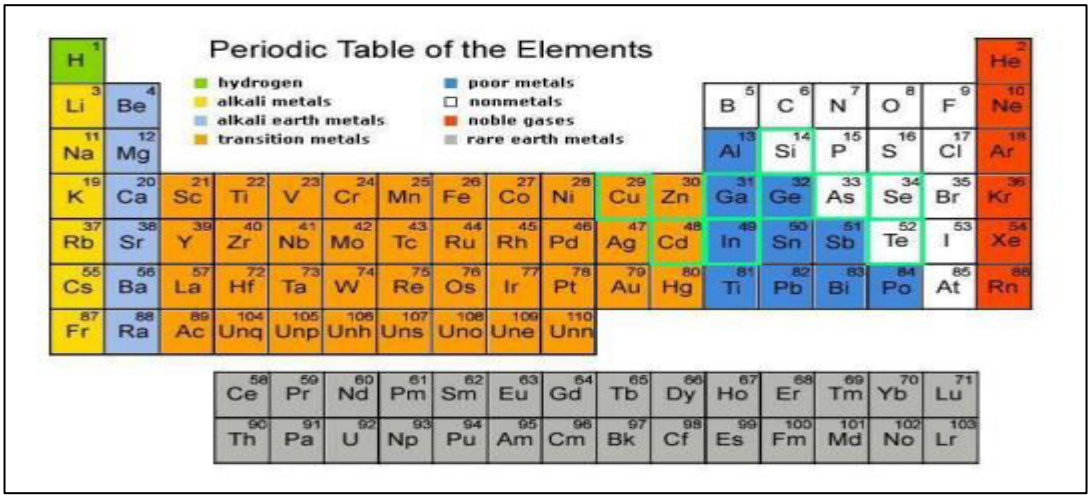


Figure 2.1. The periodic table of the element. (6)

Semiconductors, and elements used as compounds to produce semiconductors, are highlighted with green in figure.

In pure silicon crystal, the four valence electrons of a silicon atom are tied with strong covalent bonds

to four adjacent silicon atoms. Therefore at zero temperature silicon is a perfect insulator there are no free electrons to carry currents as there are in metals, but all the electrons are tied to their nuclei. As the temperature increases, some electrons gain enough energy to escape from the potential field of their nuclei and thus the conductivity of silicon increases.

According to quantum mechanics, electrons in atoms have well-defined possible, discrete energy levels. As several atoms are brought into contact these levels spread out into so called bands. Depending on the distance of the atoms and the bonds between them, there might be bands of forbidden energy called band gaps between the atoms, or the bands may overlap, forming a continuum of allowed energy states in the material. The characteristics of insulators, conductors and semiconductors depend on their band structure. (7)

The bands of interest are the valence band, that is the highest completely filled band, and the conduction band. In the valence band all the energy states are occupied and hence its electrons are immobile, whereas in the conduction band there are plenty of unoccupied states for electrons to move in response to an applied electric field. To get to the conduction band, however, an electron has to jump over a gap – the forbidden band between the valence and conduction bands. Hence the conductivity properties of a material are dependent on the size of this gap, called the band gap energy. In conductors the valence and conduction bands overlap; thus there is lots of mobile electrons to carry a current already at lower temperatures. In insulators, the band gap energy at room temperature can be 5 eV or more, and in semiconductors it is around 1 eV (at room temperature). For instance silicon has a band gap energy of 1.12 eV.

In semiconductors not only the electrons in the conduction band can move and carry currents, but also the vacancies they leave to the valence band, called holes. When an electron is excited to the conduction band, a vacant energy state, a hole, is generated to the valence band. Another electron can move into this hole, and further a third electron may move to the vacant state of the previous electron and so on. This apparent motion of holes in the valence band contributes to the current like the motion of electrons in the conduction band. When an electric field is applied, the holes in the valence band move to opposite direction with respect to the electrons in the conduction band, although the moving charge carriers are actually electrons in both bands. This feature, observed in pure semiconductors, is known as intrinsic conductivity.

Then it must be considered how an electron can obtain the required energy to jump to the conduction band. Thermally is obviously one way, but in photovoltaic the energy is received from the photons of

solar radiation. To excite an electron for instance in a silicon crystal, a photon with energy of 1.12 eV is required. The energy of a photon is related to its frequency with the following expression

$$E = h\upsilon = hc\lambda$$

Where, h is the Planck's constant (6.626 · 10−34 Js), ν is the photon's frequency (Hz), λ is its wavelength (m) and c is the speed of light (2.998 · 108 m/s). The speed of light is related to the frequency and wavelength with the expression c = νλ. Using equation (2.1) it can be calculated that in silicon photons with wavelengths shorter than 1.11 µm are able to excite an electron to the conduction band. Photons with wavelengths longer than 1.11 µm cannot do this, but their energy is wasted as heat. On the other hand, as only the exact amount of 1.12 eV is utilized by the excited electron, photons with wavelengths shorter than the limit have excess energy that also heats the cell. This means that in the case of silicon 20.2% of the sun's energy is wasted due to photons with too long, and 30.2% due to photons with too short wavelengths, giving a theoretical upper limit of 49.6% for the efficiency of a single junction silicon solar cell. In real silicon solar cells, however, the highest efficiencies that have been obtained in laboratories are in the order of 25%. The remaining 20% is lost due to various reasons, such as :

- some of the photons are reflected from the surface of the cell and some pass right through the cell
- part of the generated electron-hole pairs are recombined before they contribute to the current
- the cell has some internal resistance.

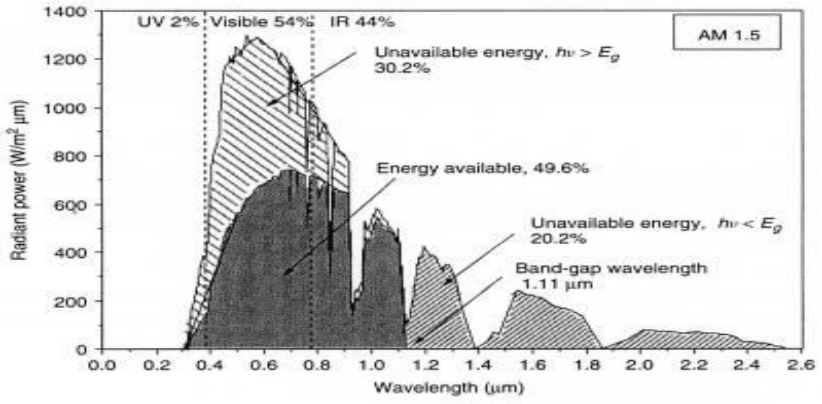


Figure 2.2.The solar spectrum at AM1.5.

In figure,dark area Indicated are the portion of the sun's energy that can be exploited by a silicon solar cell and the sparse stripesportions of energy wasted for photons with excess energy and for photons with shortage of energy

It is the size of the band gap of the material used that determines the theoretical upper limit for the efficiency of a solar cell. With lower band gap energy, there are more photons with the ability to excite electrons to the conduction band, resulting in a higher current; on the other hand, there are also more photons with excess energy that is wasted as heat. With higher band gap energy in turn, less electrons are excited, but the electrons have more energy and there are also less photons with excess energy to be dissipated. Thus, a smaller band gap yields more current and less voltage, and a higher band gap gives the opposite. The optimum band gap, that results in the highest possible power and efficiency, is estimated to be between 1.2 eV and 1.8 eV [1] – the band gap of silicon is thus slightly too small.
The Silicon properties is given below in table 2.1 (8)

Table2.1. Silicon properties is given (8)

Property	**Value**
Atomic Density	5×10^{22} cm^{-3} 5×10^{28} m^{-3}
Atomic Weight	28.09
Density (ρ)	2.328 g cm^{-3} 2328 kg m^{-3}
Energy Bandgap (E_G)	1.1242 eV
Intrinsic Carrier Concentration (n_i) at 300K*	1×10^{10} cm^{-3} 1×10^{16} m^{-3}
Intrinsic Carrier Concentration (n_i) at 25°C*	8.6×10^{9} cm^{-3} 8.6×10^{15} m^{-3}
Lattice Constant	0.543095 nm
Melting Point	1415 °C
Thermal Conductivity	1.5 $Wcm^{-1}K^{-1}$

	150 $Wm^{-1}K^{-1}$
Thermal Expansion Coefficient	2.6 x 10^{-6} K^{-1}
Effective Density of States in the Conduction Band (N_C)	3 x 10^{19} cm^{-3} 3 x 10^{25} m^{-3}
Effective Density of States in the Conduction Band (N_V)	1 x 10^{19} cm^{-3} 1 x 10^{25} m^{-3}
Relative Permittivity (ε_r)	11.7
Electron Affinity	4.05 eV
Electron Diffusion Coefficient (D_e)	kT/q μ_e
Hole Diffusion Coefficient (D_h)	kT/q μ_h

2.2. Doping

Semiconductors are very sensitive to impurities. This property can be exploited in changing their conductivity in a more favorable direction by adding suitable impurities, which is called doping. Semiconductors can be doped so that there is excess or shortage of electrons, to make n- or p-type semiconductors, respectively. When p- and n-type material is brought into contact, a p-n junction is formed.

Electrical conduction in intrinsic semiconductors is quite poor at room temperature. Semiconductors are doped to improve their conductivity and to get the required ingredients for the p-n junction:

- p--type semiconductors
- n-type semiconductors

2.2.1. P-type Semiconductor

To produce p-type semiconductor, group III elements are introduced to the semiconductor. Silicon is typically doped with boron, with approximate concentrations of one boron atom per ten million silicon atoms. Again, each boron atom substitutes a silicon atom in the silicon crystal, and is surrounded by four silicon atoms. Boron has three valence electrons that are all bound to the adjacent silicon atoms, but now an extra hole, a vacant energy state, is left next to the boron atom. This hole is easily filled by electrons from nearby atoms, and can therefore be thought as a mobile positive charge. As the hole is filled, the boron atom having a +5e charge in its nucleus is surrounded with all together

six electrons – thus a fixed ion with net charge of −e is formed. As boron atoms accept electrons, they are called acceptors. A semiconductor doped with an acceptor is called p-type semiconductor because of its free positive charge carriers.

It is important to remember that despite their names, p- and n-type semiconductors are electrically neutral. The names merely refer to the type of majority charge carriers in these materials – electrons in n-type and holes in p-type semiconductors.

2.2.2. N-type Semiconductor

N-type silicon is produced by introducing a small portion of some group V element, typically phosphorus, into the silicon crystal. Typically a ratio of approximately one phosphorus atom per 1000 silicon atoms is used – already this is sufficient to change the conductivity properties of silicon significantly. A phosphorus atom takes place of a silicon atom in the crystal lattice, and out of the five valence electrons of phosphorus, four are tied with covalent bonds to the adjacent silicon atoms. The fifth electron, however, is very loosely bound, and requires very little energy to be excited to the conduction band; at room temperature the fifth electron is most probably found in the conduction band. What the fifth electron then leaves behind is a +15e phosphorus nucleus surrounded by 14 electrons, i.e., an ion with a net charge of +e. This ion is fixed in the crystal lattice – hence there is a fixed net positive charge and a free electron towards each ion. As group V elements donate electrons, they are called donors. This type of semiconductor is called an n-type semiconductor because of the mobile negative charge carriers.

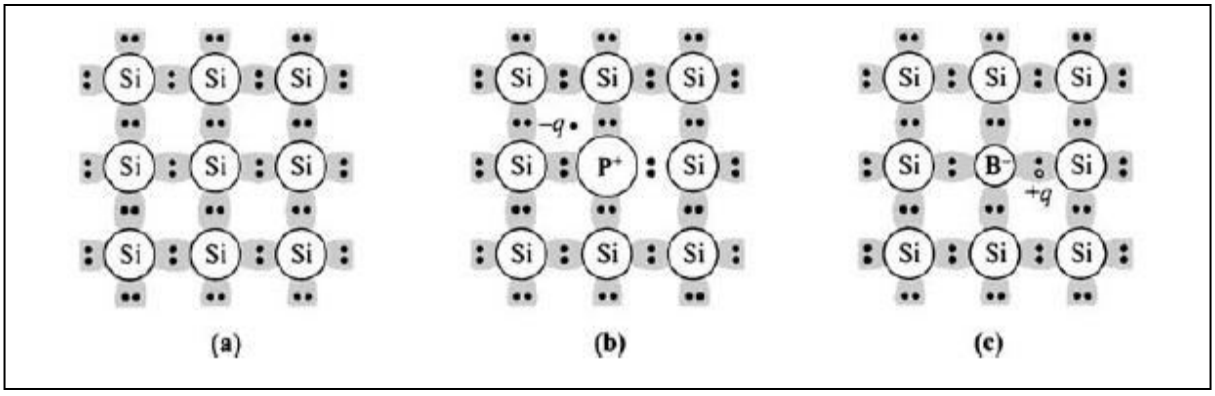


Figure 2.3.Three basic bond pictures of a semiconductor. (a) Intrinsic Si with no impurity. (b) n-type Si with donor (phosphorus). (c)p-type Si with acceptor (boron).

2.3. Orientation of monocrystalline silicon

In single crystalline silicon material the crystal orientation is defined by Miller indices. A particular crystal plane is noted using parenthesis such as (100). Silicon has a cubic symmetrical cubic structure and so (100), (010) etc are equivalent planes and collectively referred to using braces {100}. Similarly, the crystal directions are defined using square brackets, e.g. [100] and referred collectively using triangular brackets, <100>.

In solar cells the preferred orientation is <100> as this can be easily textured to produce pyramids that reduce the surface reflectivity. However, some crystal growth processes such as dendritic web <111> produce material with other orientations.

To denote the crystal directions, single crystal wafers often have flats to denote the orientation of the wafer and the doping. The most common standard is the SEMI standard:

If the minor flat is 180° from the major flat the wafer is n-type <100>

If the minor flat is 90° to the left or right the wafer is p-type <100>.

If the minor flat is 45° up on the left or right the wafer is n-type <111>

If there are no minor flats the wafer is p-type <111> (9)

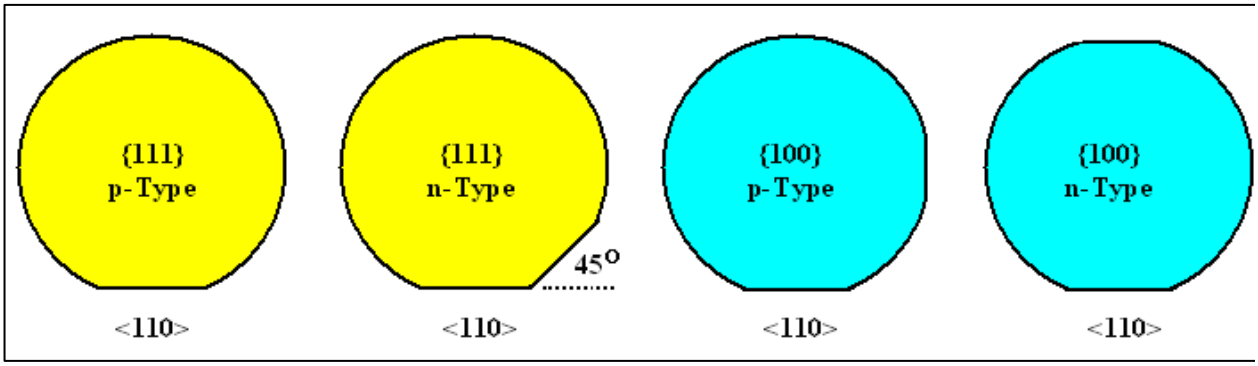


Figure 2.4. Crystal orientation of monocrystalline silicon (10)

2.4. P-N Junction for diode and solar cell

P-n junction diodes form the basis not only of solar cells, but of many other electronic devices such as

LEDs, lasers, photodiodes and bipolar junction transistors (BJTs). A p-n junction aggregates the recombination, generation, diffusion and drift effects.

P-n junctions are formed by joining n-type and p-type semiconductor materials, as shown below. Since the n-type region has a high electron concentration and the p-type a high hole concentration, electrons diffuse from the n-type side to the p-type side. Similarly, holes flow by diffusion from the p-type side to the n-type side. If the electrons and holes were not charged, this diffusion process would continue until the concentration of electrons and holes on the two sides were the same, as happens if two gases come into contact with each other. However, in a p-njunction, when the electrons and holes move to the other side of the junction, they leave behind exposed charges on doping atom sites, which are fixed in the crystal lattice and are unable to move. On the n-type side, positive ion cores are exposed. On the p-type side, negative ion cores are exposed. An electric field ε forms between the positive ion cores in the n-type material and negative ion cores in the p-type material. This region is called the "depletion region" since the electric field quickly sweeps free carriers out, hence the region is depleted of free carriers. A built in potential V_{bi} due to ε is formed at the junction.

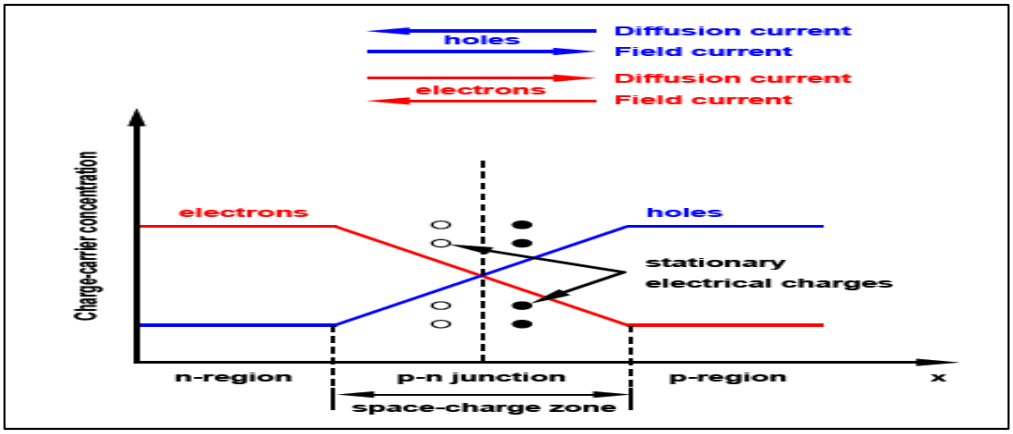


Figure 2.5.Charge carrier distribution at p-n junction and currents through the junction (11)

The diode equation gives an expression for the current through a diode as a function of voltage. The Ideal Diode Law, expressed as:

$I = I_0\left(e^{\frac{qv}{kT}} - 1\right)$ [11]

Where, I =the net current flowing through the diode

I_0 = dark saturation current

v=applied voltage across the terminals of the diode

q= absolute value of electron charge

k = Boltzmann's constant

T = absolute temperature (K)

The "dark saturation current" (I_0) is an extremely important parameter which differentiates one diode from another. I_0 is a measure of the recombination in a device. A diode with a larger recombination will have a larger I_0.

For actual diodes, the expression becomes:

$$I = I_0 \left(e^{\frac{qv}{nkT}} - 1 \right) \qquad (12)$$

Where,

n = Ideality factor, a number between 1-2

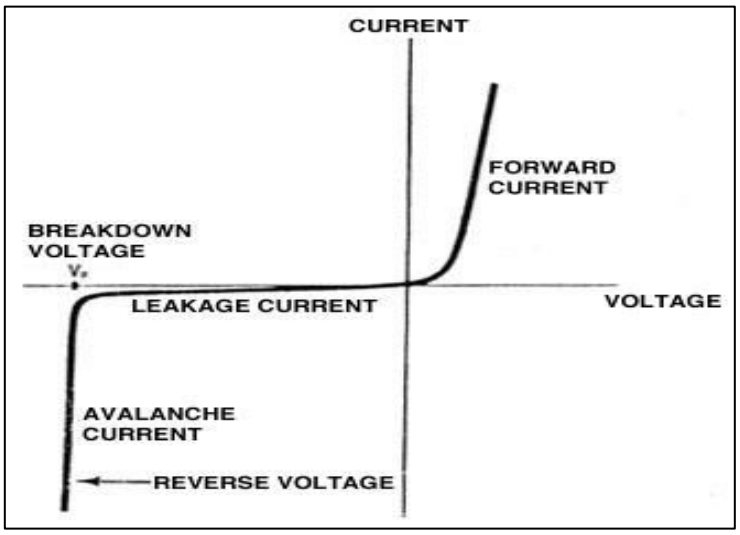


Figure 2.6. I-V Characteristics curve of an ideal p-n junction diode (13)

The collection of light-generated carriers does not by itself give rise to power generation. In order to generate power, a voltage must be generated as well as a current. Voltage is generated in a solar cell by a process known as the photovoltaic effect. The collection of light-generated carriers by the p-n junction causes a movement of electrons to the n-type side and holes to the p-type side of the junction.

Under short circuit conditions, there is no buildup of charge, as the carriers exit the device as light-

generated current. However, if the light-generated carriers are prevented from leaving the solar cell, then the collection of light-generated carriers causes an increase in the number of electrons on the n-type side of the p-n junction and a similar increase in holes in the p-type material. This separation of charge creates an electric field at the junction which is in opposition to that already existing at the junction, thereby reducing the net electric field. Since the electric field represents a barrier to the flow of the forward bias diffusion current, the reduction of the electric field increases the diffusion current. A new equilibrium is reached in which a voltage exists across the p-n junction. The current from the solar cell is the difference between load current and the forward bias current.

Under open circuit conditions, the forward bias of the junction increases to a point where the light-generated current is exactly balanced by the forward bias diffusion current, and the net current is zero. The voltage required to cause these two currents to balance is called the open-circuit voltage.

2.5. Parameters for efficiency test

2.5.1. I-V Curve

The I-V curve of a solar cell is the superposition of the I-V curve of the solar cell diode in the dark with the light-generated current. The light has the effect of shifting the I-V curve down into the fourth quadrant where power can be extracted from the diode. Illuminating a cell adds to the normal dark currents in the diode so that the diode law becomes:

$$I = I_0 \left[exp\left(\frac{qv}{nkT}\right) - 1 \right] - I_L \quad (14)$$

Where I_L = light generated current.

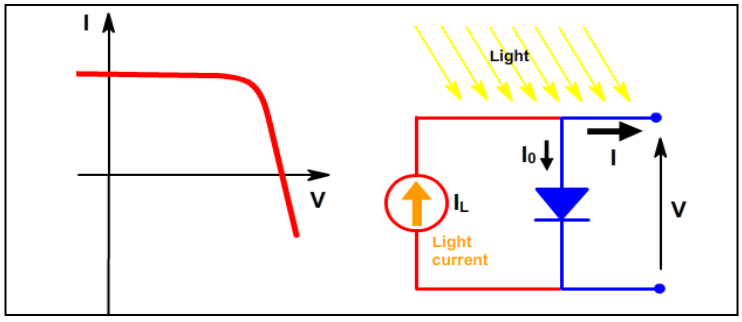


Figure 2.7.The effect of light on the current-voltage Characteristics of a p-n junction

Note: Since the cell is generating power the convention is to invert the current axis

2.5.2. Short-Circuit Current

The short-circuit current is the current through the solar cell when the voltage across the solar cell is zero (i.e., when the solar cell is short circuited). Usually written as I_{SC}, the short-circuit current is shown on the I-V curve in the figure. The short-circuit current is due to the generation and collection of light-generated carriers. For an ideal solar cell at most moderate resistive loss mechanisms, the short-circuit current and the light-generated current are identical. Therefore, the short-circuit current is the largest current which may be drawn from the solar cell.

The short-circuit current depends on a number of factors which are described below:

- the area of the solar cell - To remove the dependence of the solar cell area, it is more common to list the short-circuit current density (J_{sc} in mA/cm^2) rather than the short-circuit current the number of photons - Isc from a solar cell is directly dependant on the light intensity as discussed in Effect of Light Intensity
- the spectrum of the incident light - For most solar cell measurement, the spectrum is standardized to the AM1.5 spectrum the optical properties of the solar cell
- the collection probability - the collection probability of the solar cell which depends chiefly on the surface passivation and the minority carrierlifetime in the base (15)

2.5.3. Open-Circuit Voltage

The open-circuit voltage, V_{OC} is the maximum voltage available from a solar cell, and this occurs at zero current. The open-circuit voltage corresponds to the amount of forward bias on the solar cell due to the bias of the solar cell junction with the light-generated current. The open-circuit voltage is shown on the I-V curve in the figure.

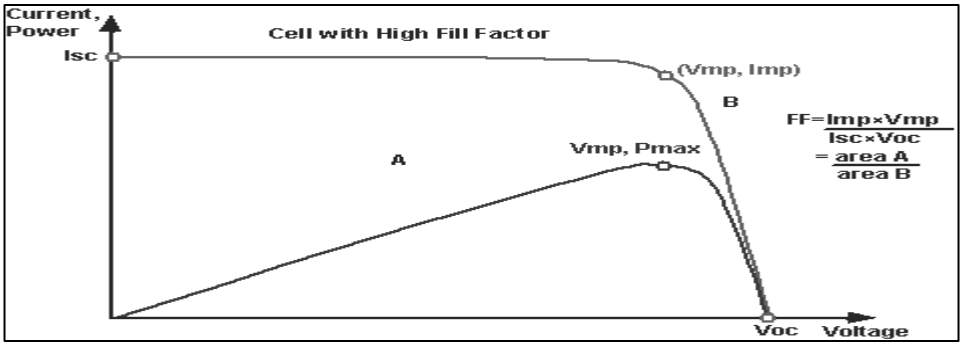


Figure 2.8. I - V curve of a solar cell showing the short-circuit current, open-circuit Voltage, fill factor 'FF', maximum power point (V_{mp}, I_{mp}) (16)

2.5.4. Fill Factor

The short-circuit current and the open-circuit voltage are the maximum current and voltage respectively from a solar cell. However, at both of these operating points, the power from the solar cell is zero. The "fill factor" more commonly known by its abbreviation "FF" is a parameter which, in conjunction with V_{oc} and I_{sc} determines the maximum power from a solar cell. The FF is defined as the ratio of the maximum power from the solar cell to the product of V_{oc} and I_{sc}. Graphically, the FF is a measure of the "squareness" of the solar cell and is also the area of the largest rectangle which will fit in the I-V curve. The FF is illustrated.The FF is most commonly determined from measurement of the IV curve and is defined as the maximum power divided by the product of I_{sc}*V_{oc}

$$FF = \frac{V_{mp} I_{mp}}{V_{oc} I_{sc}}$$

2.5.5. Efficiency

The efficiency is the most commonly used parameter to compare the performance of one solar cell to another. Efficiency is defined as the ratio of energy output from the solar cell to input energy from the sun. In addition to reflecting the performance of the solar cell itself, the efficiency depends on the spectrum and intensity of the incident sunlight and the temperature of the solar cell. Therefore, conditions under which efficiency is measured must be carefully controlled in order to compare the performance of one device to another. Terrestrial solar cells are measured under AM1.5 conditions and at a temperature of 25°C. Solar cells intended for space use are measured under AM0 conditions.The efficiency of a solar cell is determined as the fraction of incident power which is

converted to electricity and is defined as: Efficiency, $n = \frac{P_{max}}{P_{in}}$

Where, $P_{max} = V_{oc} I_{sc} F$ (17)

2.6. Effect of few parameters

2.6.1. Characteristic Resistance

The characteristic resistance of a solar cell is the output resistance of the solar cell at its maximum power point. If the resistance of the load is equal to the characteristic resistance of the solar cell, then the maximum power is transferred to the load and the solar cell operates at its maximum power point. It is a useful parameter in solar cell analysis, particularly when examining the impact of parasitic loss mechanisms. The characteristic resistance is shown in the figure 2.8.

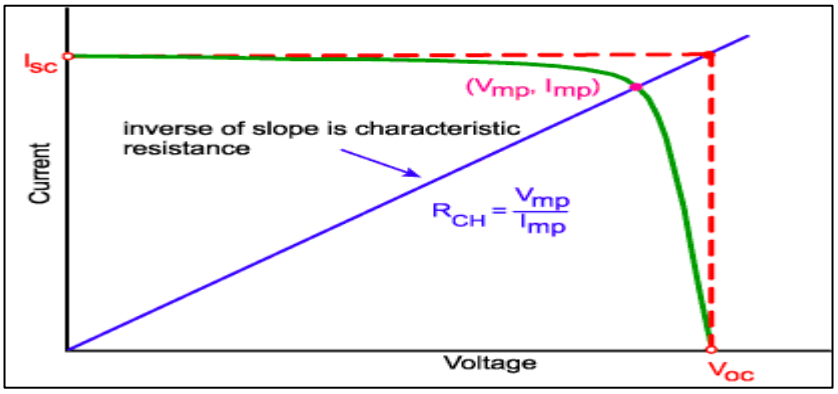


Figure 2.9. The characteristic resistance of a solar cell (18)

The characteristic resistance of a solar cell is the inverse of the slope of the line, shown in the figure above, can be given as:

$R_{CH} = \frac{V_{MP}}{I_{MP}} = \frac{V_{oc}}{I_{sc}}$

The equation for the characteristic resistance is:

$I = \frac{1}{R_{CH}} V$

Substituting the point I_{sc} and V_{oc} in the equations gives:

$I_{SC} = \frac{1}{R_{CH}} V_{oc}$

2.6.2. Effect of Parasitic Resistances

Resistive effects in solar cells reduce the efficiency of the solar cell by dissipating power in the resistances. The most common parasitic resistances are series resistance and shunt resistance. The inclusion of the series and shunt resistance on the solar cell model is shown in the figure 2.9.

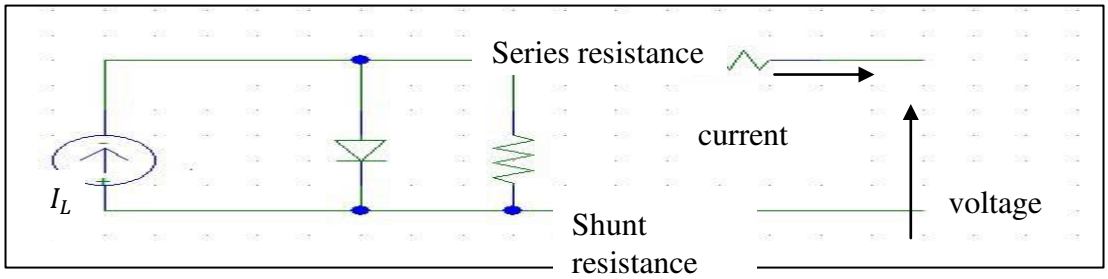


Figure 2.10. Parasitic resistances in a solar cell circuit

In most cases and for typical values of shunt and series resistance, the key impact of parasitic resistance is to reduce the fill factor. Both the magnitude and impact of series and shunt resistance depend on the geometry of the solar cell, at the operating point of the solar cell. Since the value of resistance will depend on the area of the solar cell, when comparing the series resistance of solar cells which may have different areas, a common unit for resistance is in Ωcm^2 [20]. This area-normalized resistance results from replacing current with current density in Ohm's law as shown below:

$$R'(\Omega cm^2) = \frac{V}{J} \qquad (19)$$

2.6.2.1. Series Resistance

Series resistance in a solar cell is due to three causes. Firstly, the movement of the current through the emitter and base of the solar cell. Secondly, the contact resistance between the metal contact and the silicon. Finally, the resistance of the top and rear metal contacts. The main impact of series resistance is to reduce the fill factor, although excessively high values may also reduce the short-circuit current. The effect of the series resistance on the IV curve is shown in figure – 2.13. Series resistance does not affect the solar cell at open-circuit voltage since the overall current flow through the solar cell, and therefore through the series resistance is zero. However, near the open-circuit voltage, the I-V curve is strongly affected by the series resistance. A straight-forward method of estimating the series resistance from a solar cell is to find the slope of the I-V curve at the open-circuit voltage point.

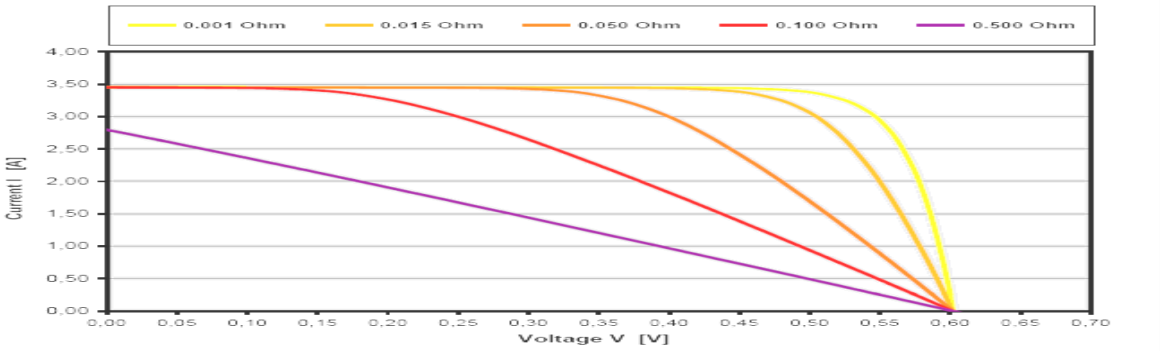


Figure 2.11. I-V curve for different series resistances

2.6.2.2. Shunt Resistance

Significant power losses caused by the presence of a shunt resistance are typically due to manufacturing defects, rather than poor solar cell design. Low shunt resistance causes power losses in solar cells by providing an alternate current path for the light-generated current. Such a diversion reduces the amount of current flowing through the solar cell junction and reduces the voltage from the solar cell. The effect of a shunt resistance is particularly severe at low light levels, since there will be less light-generated current. The loss of this current to the shunt therefore has a larger impact. In addition, at lower voltages where the effective resistance of the solar cell is high, the impact of a resistance in parallel is large.

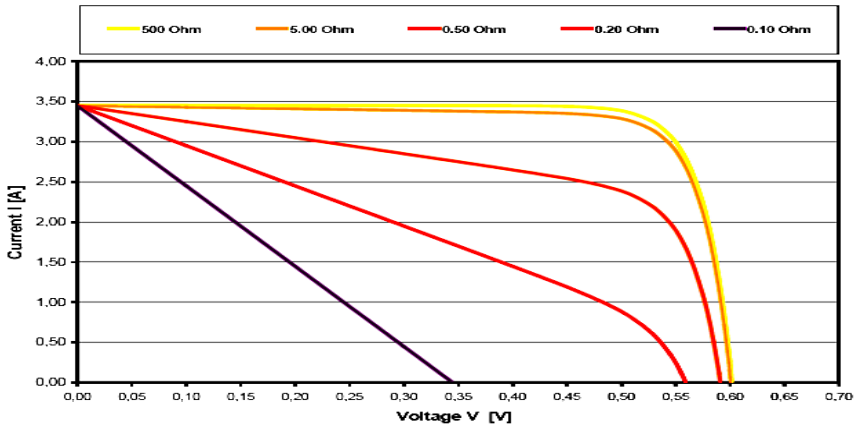


Figure 2.12. I-V curve for different parallel resistances

2.7. Effect of Temperature

Like all other semiconductor devices, solar cells are sensitive to temperature. Increases in temperature reduce the band gap of a semiconductor, thereby effecting most of the semiconductor material parameters. The decrease in the band gap of a semiconductor with increasing temperature can be viewed as increasing the energy of the electrons in the material. Lower energy is therefore needed to break the bond. In the bond model of a semiconductor band gap, reduction in the bond energy also reduces the band gap. Therefore increasing the temperature reduces the band gap.

In a solar cell, the parameter most affected by an increase in temperature is the open-circuit voltage. The impact of increasing temperature is shown in the figure – 2.12.

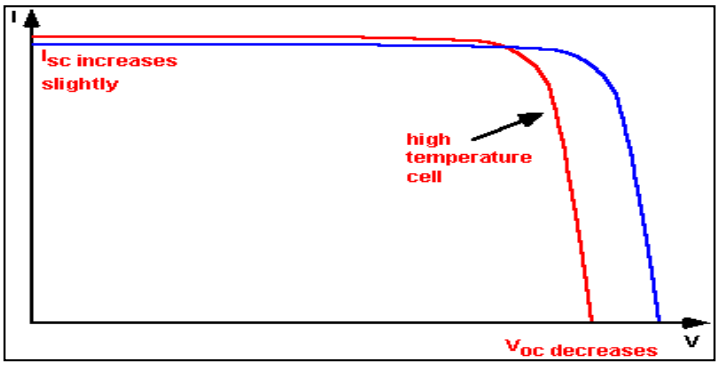


Figure 2.13. Effect of temperature on the IV characteristics of a solar cell (20)

2.8. Effect of Light Intensity

Changing the light intensity incident on a solar cell changes all solar cell parameters, including the short-circuit current, the open-circuit voltage, the FF, the efficiency and the impact of series and shunt resistances. The light intensity on a solar cell is called the number of suns, where 1 sun corresponds to standard illumination at AM1.5, or 1 kW/m^2 [16]. For example a system with 10 kW/m^2[16] incident on the solar cell would be operating at 10 suns, or at 10X (21). A PV module designed to operate under 1 sun conditions is called a "flat plate" module while those using concentrated sunlight are called concentrators.

Chapter 3

Monocrystalline Solar Cell Fabrication

3.1. Introduction

The fabrication of our silicon solar cell starts with a 200µm thick, (100) oriented Czochralski Si (or Cz-Si) wafer. The majority of silicon solar cell production is currently based upon a very standardized process that is intended to make a p-n-electrical junction on the entire front surface of the wafer and a full-area aluminum-based metallization on the back (22).The wafers generally have micrometer sized surface damages that need to be removed. After the damage removal, the wafer surface shows high optical reflectivity, for which an anti-reflection coating (ARC) is necessary. Furthermore, the top surface was textured by chemical etching before an ARC was deposited.

For a p-type crystalline silicon (c-Si) substrate, an n-type top layer while for an n-type c-Si substrate a p-type top layer acts as emitter. A thermal diffusion is commonly used for emitter diffusion (23). After the emitter diffusion, the edge isolation was carried out, as otherwise the top and the bottom surfaces of the wafers remain electrically shorted. A suitable thin dielectric coating at the front and back of the wafers were given to passivate surface defects. As the wafer becomes covered with a dielectric layer, an electrical connection to the cell becomes necessary. Ag and Al metal electrodes were formed by using screen printing of Al pastes and co-firing at a suitable temperature.

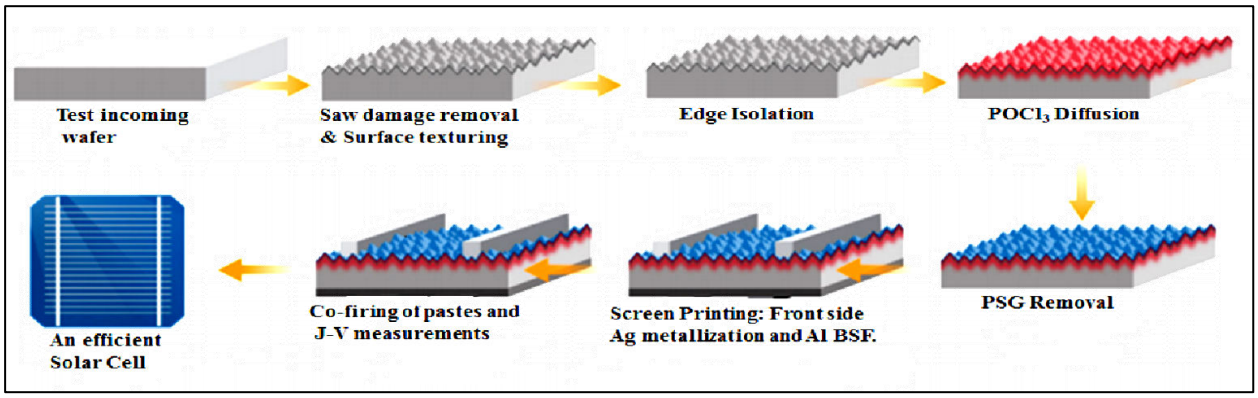


Figure 3.1. Steps of solar cell fabrication process (24)

3.2. Fabrication Steps

3.2.1. Test Incoming Wafer

Wafers are typically received from multiple supply sources, and because they can be damaged during sawing and shipping, all incoming wafers should be tested to ensure that they would provide a foundation for acceptable cell efficiencies (25).

3.2.2. Saw Damage Removal

In a solar cell, contribution from both the surface and volume of the wafer are needed. Therefore, cleaning of Si wafers is essential in order to remove the organic and inorganic contaminants from the c-Si wafer surfaces.

Wet-chemical treatments are an important step in the silicon solar cells fabrication. Process carried out in wet-chemical bench is called Etching. We have used some standard process called Radio Corporation America (RCA) cleaning.

Process 1

The surface damages to the wafers were removed by using RCA cleaning process consists of two steps normally referred to as standard cleaning 1 (SC1) and standard cleaning 2 (SC2).

The SC1 step consisting of a NH4OH/H2O2/H2O mixture, aims at organic particle removal.

For SC2 step, HCl/H2O2/H2O mixture is used to remove metal or inorganic contaminants. Figure 1 show the DI water rinsing as first step in cleaning process. Figure 2 show the wafers dip into the nitric acid solution and start the RCA clean process.

Figure 3.2.RCA cleaning process: DI water dip(left),cleaning process: Nitric Acid solution(Right)

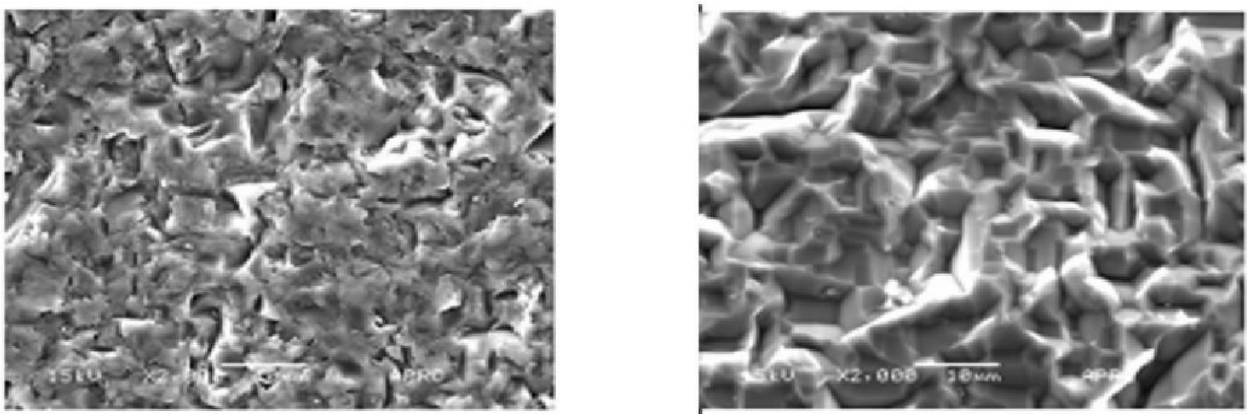
Process 2

The surface damages to the wafers were removed through isotropic etching with a concentrated solution of NaOH in de-ionized water (DI-W). DI-W helps the NaOH to break in Na+ and OH^- ions in the solution. A 10% NaOH solution, at 70°C temperature for about 10 minutes of etching removes the organic contaminants.

3.2.3. Hydrophobic Process

Saw damage removal step etches out about 5 micro meter Si from wafer surface. After that the wafers were rinsed in DI-W for 1 min, HF (2%) for 1 min, DI-W for 1 min.After that the wafers are dried using compressed air or nitrogen blow so that they are prepared for the next step.

Figure 3.3 shows the Scanning Electron Microscopic (SEM) images of raw wafer and saw damage removed wafer (26)



(a). Raw wafer (b). Saw damage removed surface

Figure 3.3. Comparison of SEM image of the (a) raw wafer and (b) saw damage removed wafer

3.2.4. Surface Texturing Process

Surface texturing is used to enhance the amount of light absorbed into devices by reducing reflection losses. In addition, surface texturing scatters light inside the semiconductor in order to trap it inside the wafer, and therefore increases the short circuit as well as the efficiency of the solar cells. KOH/IPA texturing process is used to create random pyramid features on wafer surface to reduce reflection and enhance light absorption.

For this process, a wet bench chemical treatment was utilized to etch away between 5 and 15µm of silicon wafer from the top surface. The characteristics of the etching depend upon, time of etching,

etching rate, temperature, components of the solution and its concentration. IPA enhances surface diffusion, so a rapid etching can take place in presence of IPA in the solution (27). With the alkali metal only being a spectator ion, the etching reaction proceeds as follows (28):

$$Si + 2KOH + H_2O\ K_2\ SiO_3 + 2H_2$$

The potassium silicate (K2SiO3) is soluble in water and thus silicon surface remains devoid of any deposition. For texturing process, we prepared a solution using the ratio of, KOH: IPA: H2O = 1 gram: 5 ml: 125 ml.

Initially DI water was transferred to a clean beaker and then KOH pellet was added to the beaker. The solution was then heated and when it reached at 70°C temperature, we dipped the silicon wafer and added IPA into that solution. After 10 minutes the wafers ware removed from the beaker and rinsed with DI-water then the hydrophobic process was repeated and finally the wafers ware dried using the compressed air.

Figure 3.4. After Clean Wafers in Texturing process

Figure 3.5. Compress air gun for wafer drying

3.2.4.1. Result

SEM image/ structural characterization of textured sample:

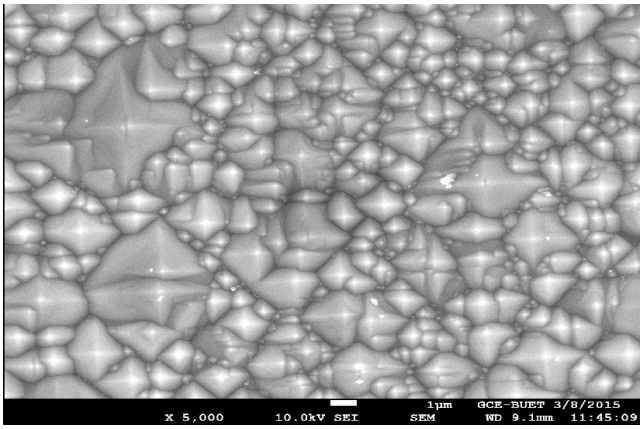


Figure 3.6. SEM of the p-type textured silicon wafer

In this anisotropic texturing process both faces of the wafer covers by micrometer sized four sided pyramids. Pyramids are of [111] planes. That means [111] planes formed on [100] oriented surface.

3.2.5. Phosphorus Diffusion Process

Forboron doped p-type silicon substrate, an n-type top layer acts as emitter. A thermal diffusion is commonly used for emitter diffusion (29) (30). Phosphorus (P) diffusion is currently the primary method for emitter fabrication in silicon (Si) solar cell processing (31) (32). Along with nitrogen (N2) and oxygen (O2) gases, phosphorus oxy-chloride (POCl3), a liquid source of phosphorus, is also widely used in the standard diffusion process of solar cells (33) (34).The diffusion depends on various factors, of which temperature and gaseous environment is most important (35) (36). In oxygen environment and at high temperature, phosphorus diffusion leads to formation of n+ type emitter at the top surface of the wafer.

The diffusion was carried out in two stages, pre-deposition and drive-in (37) The formation of phosphorous-rich oxide films, phosphor silicate glass (PSG), on the silicon substrate carry out at pre-deposition stage and in drive-in stage, the phosphorous-rich oxide film acts as an infinite source for phosphorous diffusion into the Si substrate. The phosphorus atoms formed at the PSG-Si interface penetrate through the silicon wafer and can be simplified with the following reaction equations:

pre-deposition:

$POCl_3$ (liquid) + N_2 (bubble) → POCl3 (vapor)

$POCl_3 + 3O_2 \rightarrow 2\ P_2O_5 + 6Cl2$

drive-in:

$2\ P_2O_5 + 5Si \rightarrow 4P + SiO_2$

P + 3Si → n-type doped Si

Diffusion steps:

i. At first the wafers are put inside the diffusion chamber with an initial temperature is 600°C.
ii. Then turn ON N_2 gas and wait for 10 minutes.
iii. Then increase the temperature to 875°C keeping N_2gas turn ON.
iv. When temperature reach at 875°C turn OFF N_2 gas, turn ON 0_2gas and $POC1_3$ simultaneously.
v. This process continues for 10 minutes.
vi. Then turn OFF 0_2 gas and $POC1_3$ simultaneously and turn ON N2.
vii. After that wait for 10 minutes.
viii. Then turn OFF N_2 and turn ON 0_2 and wait for 10 minutes.
ix. Again turn OFF 0_2 and Turn ON N_2gas and wait for 10 minutes.
x. Then reduce the temperature to 600°c keeping N_2 turn ON.
xi. At 600°c, turn OFF N_2 gas.

Figure 3.7. The phosphorus doped silicon wafer

In presence of oxygen, phosphor silicate glass (PSG) is formed at the 850°C temperature. Phosphor silicate glass or PSG isphosphorus doped silicon dioxide, a hard material layer formed at the top surface of Si wafer in the pre-deposition stage of diffusion process . In the drive-in stage, a deeper junction was formed as phosphorus atoms from the PSG layer diffuse deeper, thus thicker emitter and a lower surface concentration of dopant was achieved. But a thin PSG layer was still present on top of the wafer after drive-in stage of diffusion. Due to this thin phosphor silicate glass (PSG) layer the top wafer surface becomes glassy and degrade blue response of solar cells. To remove the PSG layer we prepared a 10% hydrofluoric acid (HF) solution and then dipped the silicon wafer for one minute after that the wafer were rinsed with DI-water.

3.2.6 Edge Isolation

A critical step in solar cell fabrication is electrical isolation of n and p type regions. Edge isolation is done to separate front side and back side. By using an acid barrier paste with the help of screen printing to isolate the edge. After the screen printing is done the wafers are dried for 10 minutes in a preheated oven at 200 °C. Figure 3.7(a) shows a screen printer used and (b) screen printing dice

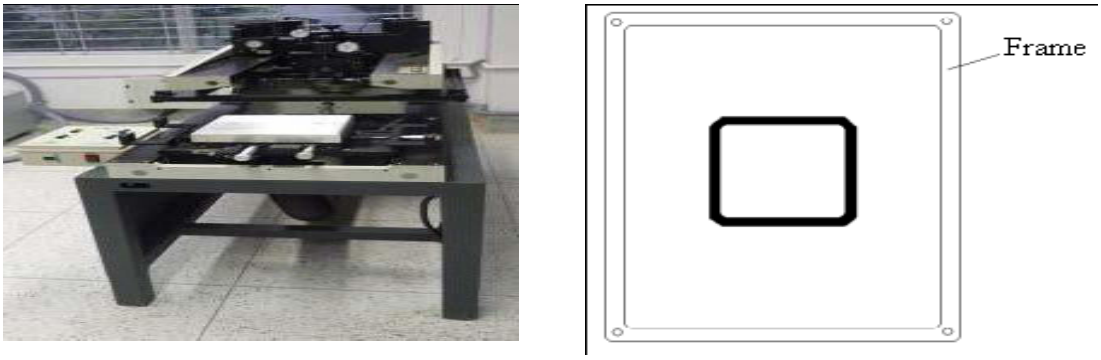


Figure 3.8. (a) Screen printer (b) screen printing frame

3.2.7 Back and front contact /surface metallization

Screen printing process is most commonly used to form metal contacts on back and front surfaces of solar cells. It is cost effective, robust, simple, inexpensive, and fast method of metallization of the solar cells [17][18]. The screen printing of Ag and Al pastes for the formation of the front and rear electrical contacts has been in use by the silicon industrial community since the 1970s. At the front surface the metallization creates electrical connection to thin n+ layer whereas at the back surface it provides an

electrical connection and at the same time it creates a p+ layer. Chemicals are Ferro FX53-038, aluminum type for rear surface and Ferro CN33-462, silver type for front surface. The screen is made up of an interwoven mesh kept at a high tension, with an organic emulsion layer defining the printing pattern. Figure 3.10 shows a microscopic image of the screen and the screen mask. An H-pattern screen that was mounted in an aluminum frame was then overlain on the front side of the cell and the metallization paste was squeezed over the wafer surface with a screen printer.

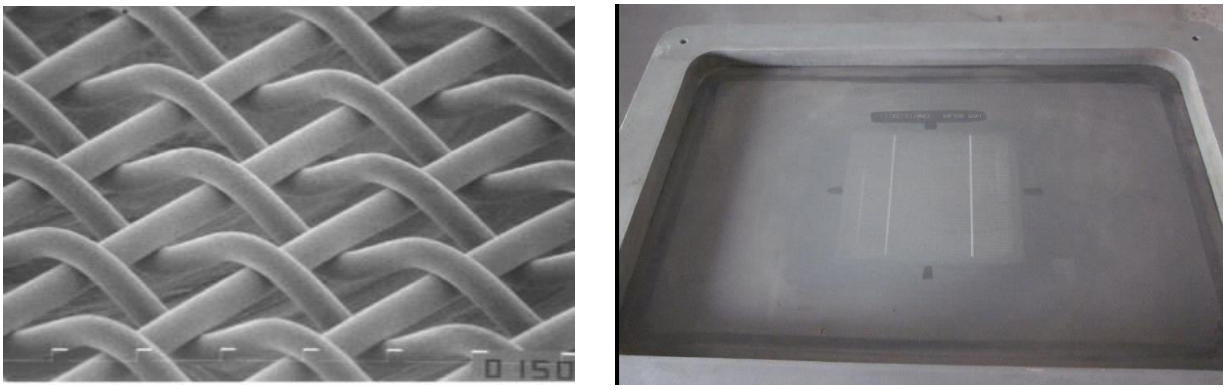


Figure 3.9. a) Microscopic image of the screen b) Image of front side printing mask

After every steps of screen printing, the silicon wafers are required to go through drying at relatively low temperature for certain period in a preheated oven at 120°C for 10 minutes so that the paste gets attached well to the wafer surface.

3.2.8 Co-firing by rapid thermal annealing

In order to establish an ohmic contact (low resistive contacts), contact firing is recommended in silicon solar cell processing. In this case, a belt conveyer system integrated RTA processing unit is used for a continuous processing of contact firing. A conveyor belt furnace capable of reaching 1000 °C temperature. RTA of screen printed cells is done at a temperature of 500, 600 and 800 °C respectively. The wafers are passed through a moving belt which goes inside the RTA machine. Figure 3.11 shows the contact firing process of screen printed Si solar cell.

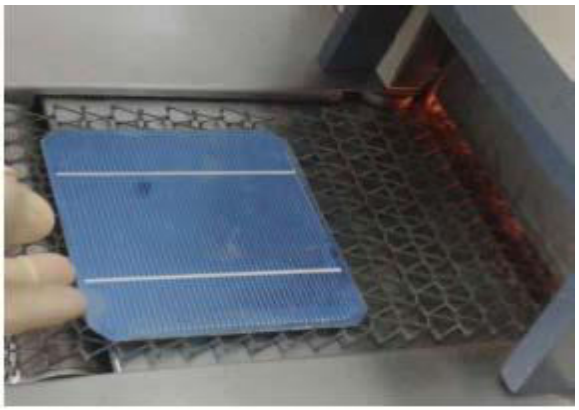


Figure 3.10. Contact firing at RTC furnace

Chapter 4
Monocrystalline Solar cell charecterization

4.1. Charecterization processes

During cell fabrication there are two processes of characterization of textured surface of Si wasfer. One is surface reflection and response (SRR) and another is scanning electron microscope (SEM). Other characterization tests are carried out, after completing the fabrication of a solar cell. These tests show the efficiency of solar cell . The major characterization equipments are LIV tester with which it was possible to evaluate the performance of the cell and mainly to calculate the efficiency of the solar cell, SPV method which relies on analyzing illumination induced changes in the surface voltage and four point probe for measuring sheet and bulk resistance of the cell.

4.2.SRR Method

Surface spectral reflection is determined by measuring the light reflected from the surface of a Si wafer or solar cell as a function of wavelength. Spectral response is determined by measuring the photo-generated I-V response of the solar cell as a function of wavelength. By a careful correlation of spectral reflection, and spectral response, solar cell internal quantum efficiency can be determined.

A simple, computer-controlled, normal incidence measurement system was designed for SRR measurements of Si wafers and solar cells. Measurement system is based on a mini monochromator driven with a stepper motor to vary wavelengths in ~ 500-1200-nm spectral range. Incident light is obliquely incident on the surface of device under test. The resulting signal is connected to a Stanford Research 510 lock-in amplifier. This system can be modified to measure spectral response as a function of wavelength as well as a function of flux density at fixed wavelength. A LabVIEW interface is used for system control and data acquisition. (38)

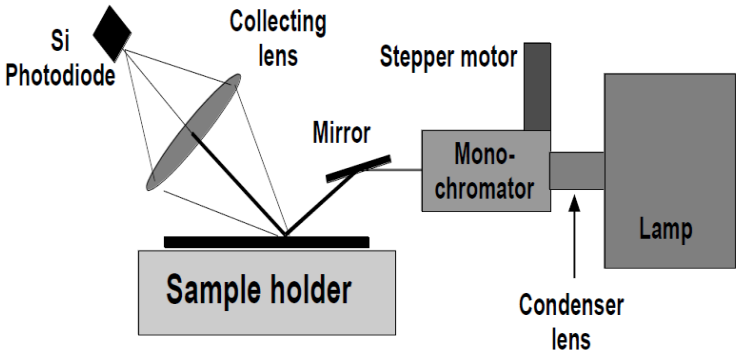


Figure 4. 1: Schematic diagram of the surface reflection and measurement system

During normal operation, light from the exit slit of the monochromator is guided to the wafer at near normal incidence. Stepper motor is used to vary monochromator output wavelength. A light chopper is placed at the exit slit of the monochromator to provide reference signal to the lock-in to ensure all the stray light is rejected by the system and enhance system sensitivity from nano-volt to mV range. Surface reflection as a function of wavelength is determined by measuring photodetector response through lock-in amplifier. In order to determine spectral response, completed solar cell with top and bottom contacts is placed on vacuum chuck. Vacuum pump is turned on to ensure low resistivity contact between wafer backside and the vacuum chuck. Current-voltage probes make contact with the front surface (Fig. 6) and the back contact is through the Au-coated wafer vacuum chuck. The lock-in output and stepper motor are controlled by a PC using a LabVIEW interface. The system wavelength range is from ~ 500-1000-nm. All data is written to a file in text form for subsequent plotting and processing.

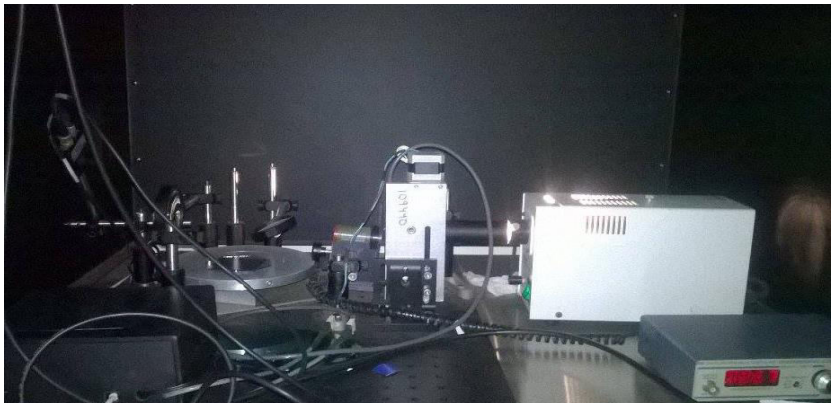
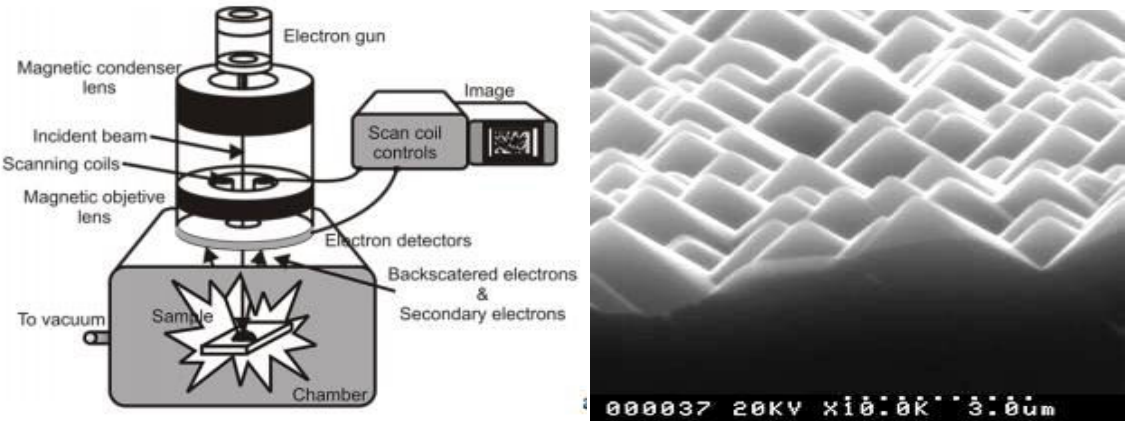


Figure 4.2: Picture of surface reflection and measurement system

4.3. SEM

The use of the texturization processes to enhance the solar cell efficiency, increasing the light

absorption and therefore the short circuit current of the solar cell, must be controlled due to the introduction of new problems in the metallic contact emplacement, poor quality contacts and hot spots. SEM is an interesting tool to control the pyramids size and the formation mechanism involved in the texturization processes. As it has been mentioned in this work, there is a correlation between the pyramids size and the macroscopic parameters as the short-current intensity. The scanning electron microscope (SEM) is a microscope that uses electrons instead of photons to form an image. This microscope, basically, consists of an electron gun and a set of electromagnetic fields to guide the electron beam toward the sample surface. Then, the beam scans the sample thanks to scanning coils. Finally, backscattered and secondary electrons received from the surface are collected by detectors and converted in a signal to produce the final image. Nowadays, the surface morphology of a solid sample can be studied by the SEM, because it has much higher resolution and has a large depth in field than a traditional microscope. On the other hand, in addition to the backscattered and secondary electrons from the sample surface, there are others types or signals produced during this process (Auger electrons, X-ray fluorescence photons and others photons with various energies) that could be used in chemical analysis. (38)



(a) (b)

Figure 4.3: Scanning electron microscope (a), SEM image of randomly textured (b) (38)

4.4. LIV Tester

LIV (Light-Current-Voltage) testing is done to evaluate the performance of the cell and mainly to calculate the efficiency of the solar cell. Initially the wafer is kept on the gold plated tray and then the bus bar of the cell is aligned with the pogo pins. Then the vacuum is turned on. Then the power supply and the control box are connected to the Laptop. LIV measurements using inexpensive, flash, xenon light source for illumination. LIV data acquisition is based on a custom-designed electronic interface integrated with high resolution, programmable voltage supply. Voltage across the solar cell is applied to measure the light generated photo-current. A user-friendly LabVIEW interface capable of writing data in ASCII format forms the basis of data acquisition. Spectral distribution of xenon high intensity

plasma discharge lamp is light is closest to the solar spectra, and is industry standard. The flash LIV system is capable of measuring small (~ 10 cm^2) and large (up to ~15x15 cm^2) solar cells. The intensity variation is controllable in ~ 10 mW/ cm2 to 100 mW/ cm2 through simple absorptive metallic filters.

Figure 4.4: LIV measurement System

Solar cells are characterized by their ability to convert sunlight into electricity. The light intensity (L)-current (I)-voltage (V) test is a series of measurements performed on complete solar cells to measure their operating characteristics. The LIV test identifies characteristics such as short circuit current (Isc), open circuit voltage (Voc), fill factor (FF) and maximum power (P_{max}). These results can be used to determine the efficiency of solar cell. Solar cells are tested under one-sun conditions using Xenon arc lamps; a xenon spectrum is closest to sunlight. Data acquisition based on programmable current-voltage source power supplies capable of handling current up to ~ 8 A is used in conjunction with a proprietary data acquisition system. Calibration of this LIV measurements system is based on independently measured c-Si solar cells at Sandia National Laboratories. (38)

4.5. SPV

The surface photovoltage (SPV) method is a well-established contactless technique for semiconductor characterization that relies on analyzing illumination-induced changes in the surface voltage. Electrical properties of a free semiconductor surface are mainly determined by surface-localized electronic states within the semiconductor band gap or double layer of a charge, known as a surface dipole. The charge transfer between bulk and surface induced by the appearance of surface-localized electronic states results in a non-neutral region named surface space charge region. If light falls on the pn-junction, the photons create electron-hole pairs separated by the space charge. Thus, in p-type silicon the majority carriers are holes, the charge in the depletion region is negative, and the electric field in the depletion region forces electrons to the surface, creating a surface photovoltage. Photons are absorbed not only in the pn-junction but also in the p-type area. The electrons produced are minority carriers in those areas and their concentration is greatly reduced by recombination. The n-layer must therefore be sufficiently thin for the electrons of diffusion length L to pass through the n-layer. i.e, L >> t,
Where t = thickness of n-layer. When a typical 300µm thick silicon wafer is illuminated by strong sunlight of irradiance 1000 mW/cm2, electrons and holes are generated at a rate of 9×1018 cm-3 s-1 .

The electric potential and the charge distribution are related to each other through the Poisson equation and the experimental value of the photovoltage coincides with the change of the surface potential. Minority carriers that drift around in the bulk either eventually recombine with majority carriers, or they reach the surface, where they produce a surface photovoltage. The shorter the diffusion length, the less likely minority carriers will make it to the surface to cause surface photovoltage. Longer wavelength light penetrates deeper into silicon than short wavelength light. Therefore, the longer wavelength will penetrate more deeply into the silicon, the minority carriers created will be more likely to recombine before they reach the surface and the longer wavelength light
will produce a smaller SPV signal than the short wavelength light .

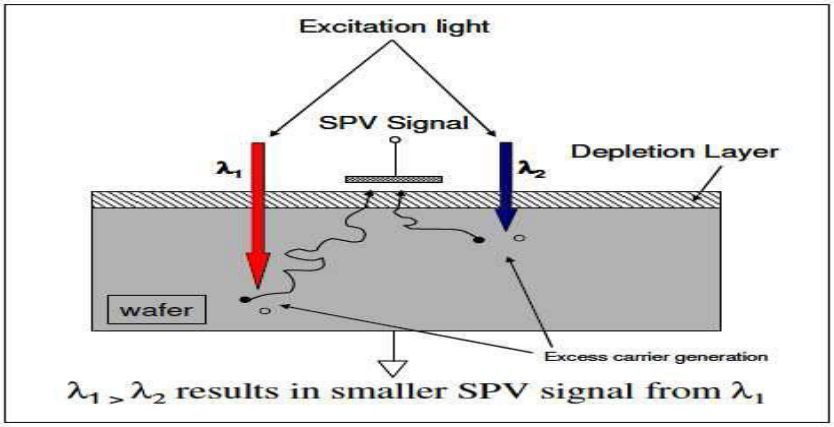


Figure 4.5: SPV Signal Changes with Penetration of incident light and wavelength

One can determine the diffusion length by comparing these two SPV signal produce by the two different wavelengths.

Methodology

A simple, computer-controlled, normal incidence measurement system was designed for SPV measurements of minority carrier diffusion length and lifetime of Si solar cell. Measurement system is based on a mini monochromator driven with a stepper motor to vary wavelengths in 400-1200-nm spectral range. Light-induced surface photovoltage (SPV) is measured as a function of the wavelength. SPV is measured using a Stanford Research 510 lock-in amplifier. This system can be modified to measure SPV as a function of wavelength as well as a function of flux density at fixed wavelength. A LabVIEW interface is used for system control and data acquisition.

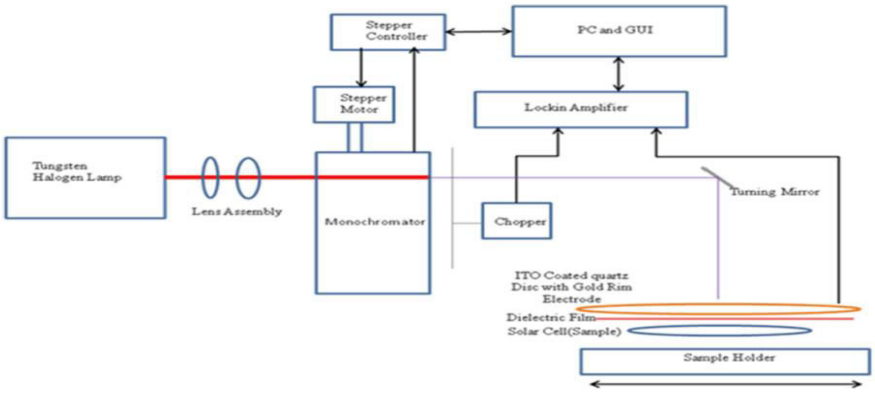


Figure 4.6: The schematic diagram of minority carrier diffusion length measurement system

Light from a tungsten-halogen lamp is focused onto the entrance slit of the monochromator. Light from the exit slit of the monochromator is guided to the solar cell at normal incidence. Stepper motor is used to vary monochromator output wavelength. A light chopper is placed at the exit slit of the monochromator to provide reference signal to the lock-in amplifier to ensure all the stray light is rejected by the system and enhance system sensitivity from nano-volt to mV range. Capacitive SPV voltage is measured by placing an ITO/Au coated quartz plate on top of the solar cell to be measured. A thin-sheet of Teflon film is placed between the top glass electrode and the solar cell to create electrical isolation. The bottom electrode is connected to the Si solar cell and is Au-coated to provide reduced contact resistance. The lock-in amplifier output and stepper motor are controlled by a PC using a LabVIEW interface. The system wavelength range is from ~ 400- 1200-nm. All data is written to a file in text form for subsequent plotting and processing (38)

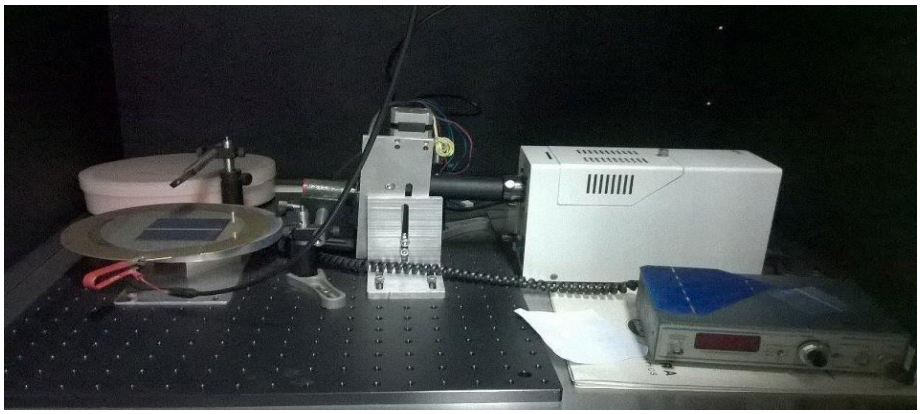


Figure 4.7: Picture of SPV Measurement system.

4.6. Four Point Probe

A four point probe is a simple apparatus for measuring the resistivity of semiconductor samples. By passing a current through two outer probes and measuring the voltage through the inner probes

allows the measurement of the substrate resistivity. The doping concentration can be calculated from the resistivity using formulas

The sheet resistivity of the top emitter layer is very easy to measure experimentally using a "four point probe". A current is passed through the outer probes and induces a voltage in the inner voltage probes. The junction between the *n* and *p* -type materials behaves as an insulating layer and the cell must be kept in the dark.

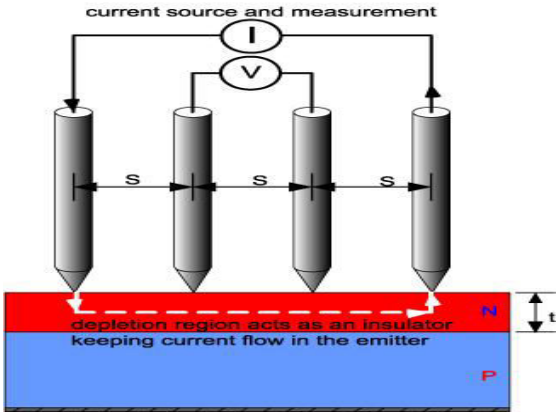


Figure 4.8: Resistance measurement by Four Point Probe (38)

Using the voltage and current readings from the probe:

$$\rho_{\square}\left(\frac{\Omega}{\square}\right) = \frac{\pi}{ln\,(2)}\frac{V}{I}$$

Where:

$$\frac{\pi}{ln2} = 4.53$$

The typical emitter sheet resistivity of silicon solar cells lies in the range 30-100 Ω/□ .

In typical usage the current is set to 4.53 mA so that the resistivity is simply the voltage reading in mV.

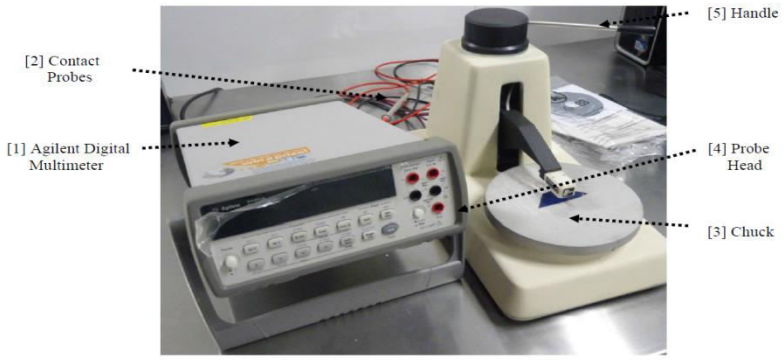


Figure 1: Four Point Probe

Figure 4.9: Four Point Probe (38)

The Measurement of Bulk Resistivity

The measurement of bulk resistivity is similar to that of sheet resistivity except that a resistivity in cm^{-3} is reported using the wafer thickness, t:

$$\rho = \frac{\pi}{ln\,(2)} t \left(\frac{V}{I}\right) = 4.523t \left(\frac{V}{I}\right)$$

Where *t* is the layer/wafer thickness in cm.

The simple formula above works for when the wafer thickness less than half the probe spacing ($t < s/2$). For thicker samples the formula becomes:

$$\rho = \frac{V}{I} \frac{\pi t}{ln\left(\frac{sinh\left(\frac{t}{s}\right)}{sinh\left(\frac{t}{2s}\right)}\right)}$$

Where *s* is the probe spacing.

Chapter 5

Experimental Process and Result Analysis

5.1. Description of Si wafers

Crystal orientation of Si wafer is <111> p type. That means there is no minor flat plate.
Size of the samples – approximately 3cm by 4cm
Thickness of raw wafer is 200µm

5.2 Etching method 1

Table 5.1: Etching process 1

No.	Solution	Time	Temperature
01	Acetone (C_3H_6O)	2 minutes	
02	Methanol(CH_4O)	2 minutes	
03	Dehydration bake in hot plate	15 minutes	80°C

This recipe was influenced by the degreasing process described in the book "handbook of semiconductor wafer cleaning" by Werner Kern. Where Ultrasonic bath was used to clean Si wafers by trichloroethylene, acetone and methanol. Trichloroethylene was not found and ultrasonic bath was not available.

5.2.1. Pictures of Samples

Figure5.1: Pictures of sample 1,2 and 3 respectively

5.3. Etching method 2

Table 5.2: Etching process 2

No.	Solution Ratio	Time	Temperature
01	NaOH : H_2O (DI) 1gm : 10 ml	10 minutes	70°C
02	DI water	1 minute	
03	HF : H_2O (DI) 1gm : 50 ml	3 minutes	
04	DI water	1 minute	

50gm : 500ml (NaOH : H_2O) was used here. This solution is a alkali base solution.

5.3.1.Pictures of Samples

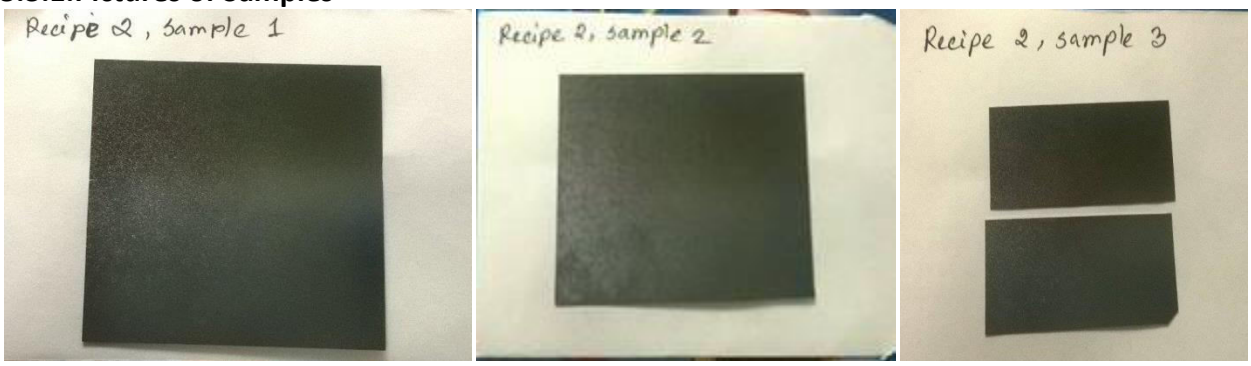


Figure5.2: Pictures of sample 1,2 and 3 respectively

5.4. Etching method 3

Table 5.3: Etching process 3

No.	Solution Ratio	Time & Temperature
1.	DI Water	1 minute

2.	DI H_2O : HF -- (50: 1)	1 minute
3.	DI Water	1 minute
4.	HNO_3 : HF -- (50: 1)	30 minutes
5.	DI Water	1 minute
6.	DI H_2O : HF -- (50: 1)	1 minute
7.	DI Water	1 minute

Plastic Jar was used in case of HF acid.IPA was added after putting the SI wafer inside the solution.
In case of HNO_3 : HF -- (50: 1), 100 ml HNO_3 and 2 ml HF were used. This solution is acidic

5.4.1.Pictures of Samples

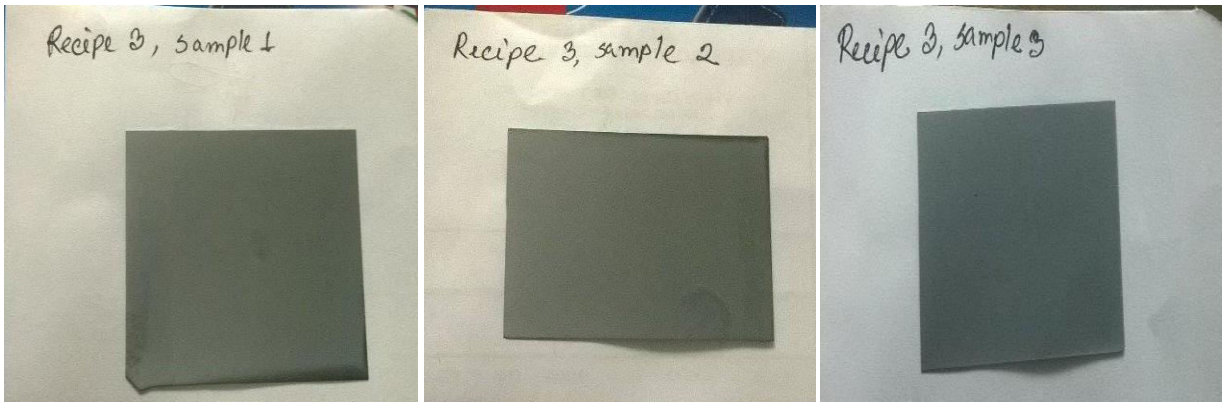


Figure5.3: Pictures of sample 1,2 and 3 respectively

5.5. Comparison among impact of three different etching methods

Table 5.4:Mass change of Samples

Sample No.	Mass change of Samples					
	Etching method 1		Etching method 2		Etching method 3	
	Before Cleaning	After Cleaning	Before Cleaning	After Cleaning	Before Cleaning	After Cleaning

1	0.74	0.74	1.42	1.24	1.03	0.99
2	0.93	0.93	1.23	1.09	0.99	0.94
3	0.64	0.64	0.70	0.62	0.85	0.79

After cleaning wafers etched by method 2 and 3 were lost masses and looked shiny but by method 1 showed no apparent changes.

Texturing and SEM image

5.6. Texturing Process

Table 5.5. Texturing process description

No.	Solution Ratio	Time	Temperature
1.	KOH : IPA : H_2O (DI) 1 gm : 5 ml : 125 ml	10 minutes	70°C
2.	DI Water	1 minute	
3.	HF:H_2O (DI) 1 gm : 50 ml	3 minutes	
4.	DI Water	1 minute	

Exhaust system was kept on. Plastic Jar was used for HF acid. 8 gram KOH, 40 ml IPA and 1000 ml H_2O were used.

5.7. Comparison among impact of three different recipes after texturing

Table 5.6: Texturing effect on mass

Sample No.	Mass change of Samples					
	Etching method 1		Recipe 2		Recipe 3	
	Before Texturing	After Texturing	Before Texturing	After Texturing	Before Texturing	After Texturing
1	0.74	0.71	1.24	1.04	0.99	1.00

2	0.93	0.89	1.09	0.96	0.94	0.93
3	0.64	0.62	0.62	0.60	0.79	0.72

After texturing wafers were lost masses and brightness. The weight of the silicon wafer before and after texturisation was measured with a high precision scale of range 0.01gm to 50gm. The measured value of weight loss was 0.03gm, 0.116gm, 0.023gm respectively. that means 0.78µm,2.3µm,0.50µm (here the thickness of raw wafer is 200 µm) silicon were removed/dissolved within 10 min during the etch processes respectively. The etch rate of silicon wafer surface using KOH/IPA solution in our experiment was 1.19 µm /min whereas the standard single side etch rate is about 2.1 µm/min.

5.8. Spectral Response of wafers

Wavelength range used 400nm-1200nm.
Step of wavelength was 15
Signal sensitivity range of the lock in amplifier was 200mv

Etching method 1

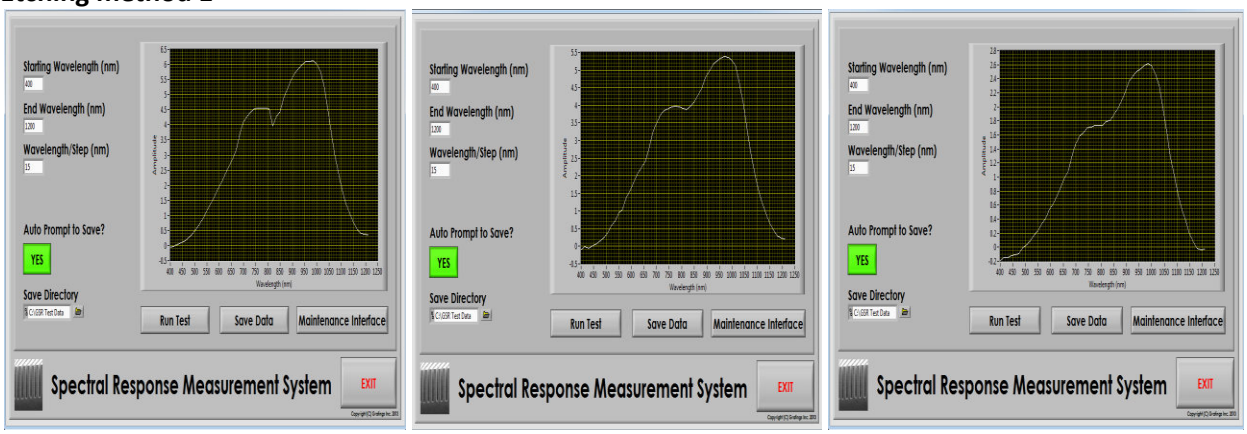


Figure 5.4: Spectral response of etching method 1 sample 1,2,3 respectively after texturing

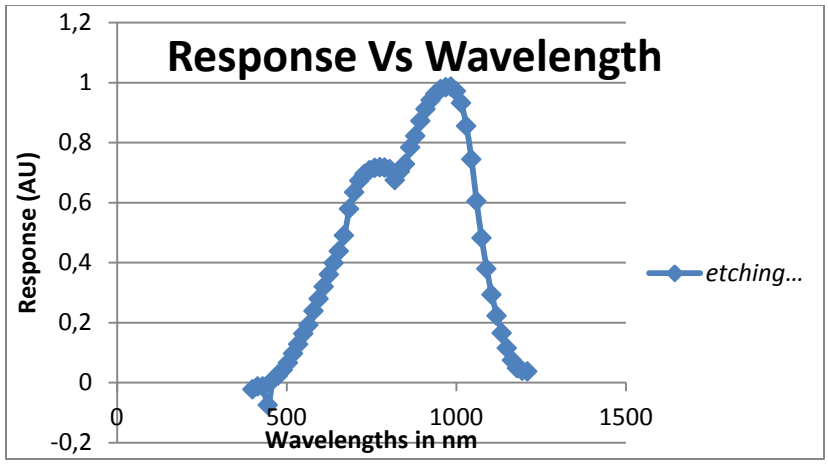


Figure5.6.: Graph of response vs wavelengths (nm) for etching method 1

This graph shows the response of textured wafer surface with the wavelength of light. The wafer surface sensitivity with light is increased with wavelength up to 715 nm after that there is a saturated value up to 820nm and then increased and reach it maximum values. From this response vs wavelength graph we can calculate the reflectivity of the textured wafer.

Etching method 2

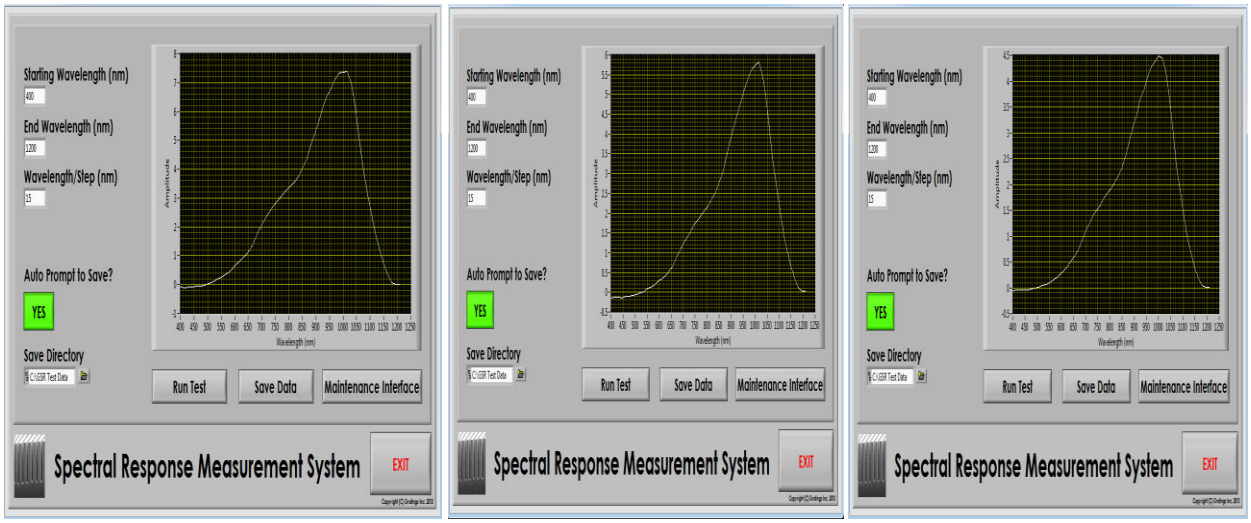


Figure 5.7: Spectral response of etching method 2, sample 1,2 and 3 after texturing respectively

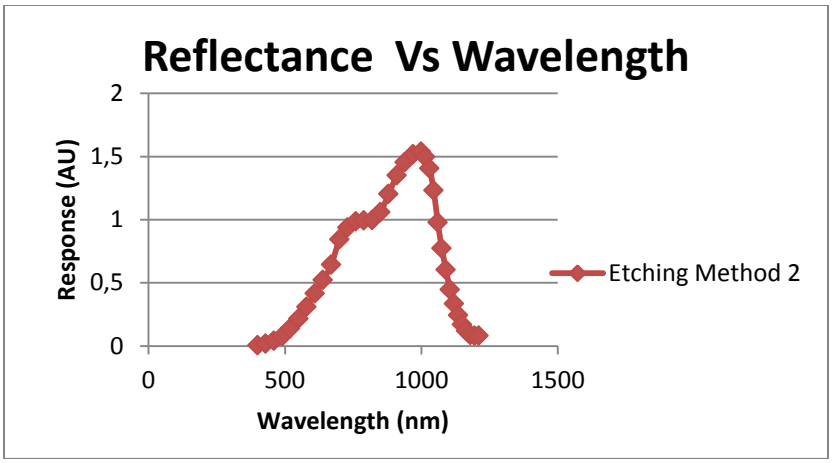


Figure5.8: Graph of response vs wavelengths (nm) for etching method 2

This graph shows the response of textured wafer surface with the wavelength of light. The wafer surface sensitivity with light is increased with wavelength up to 730 nm after that there is a saturated value up to 820nm and then increased and reach it maximum values. From this response vs wavelength graph we can calculate the reflectivity of the textured wafer.

Recipe 3

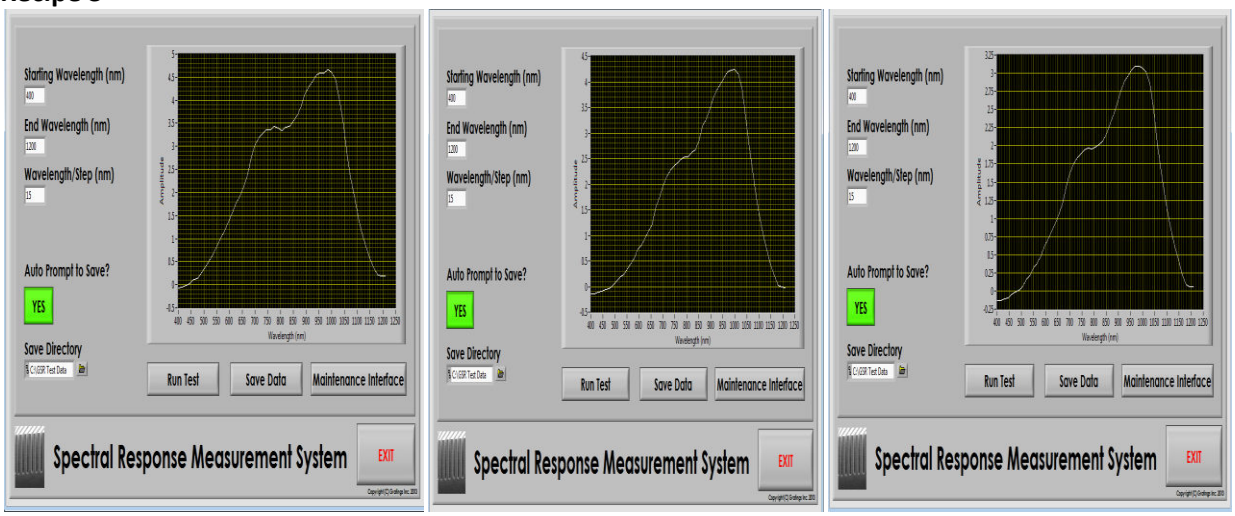


Figure 5.9: Spectral response of etching method 3, sample 1,2 and 3 after texturing respectively

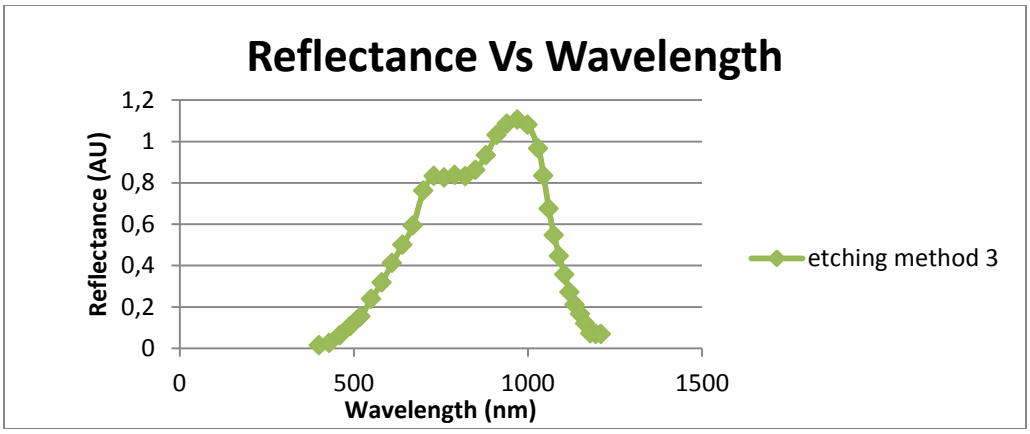


Figure5.10: Graph of average amplitude vs wavelengths (nm) for cleaning recipe 3

This graph shows the response of textured wafer surface with the wavelength of light. The wafer surface sensitivity with light is increased with wavelength up to 730 nm after that there is a saturated value up to 850nm and then increased and reach it maximum values. From this response vs wavelength graph we can calculate the reflectivity of the textured wafer.

Mirror image:

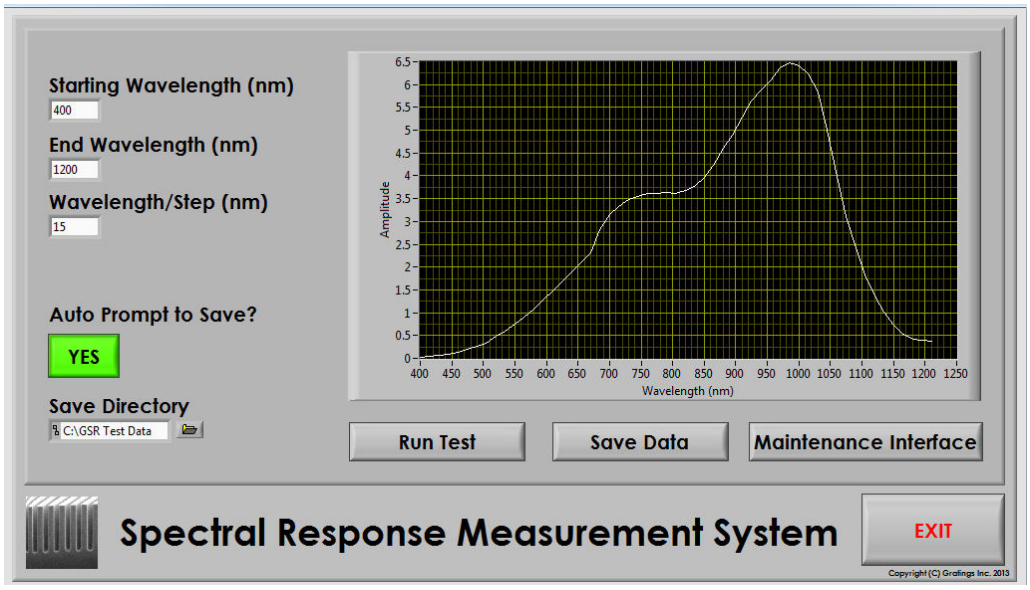


Figure5.11: Mirror image at 200mv

With mirror image as reference 100% all the response of textured wafer by three different etching methods are compared. And thus percentage reflectance is found for each method.

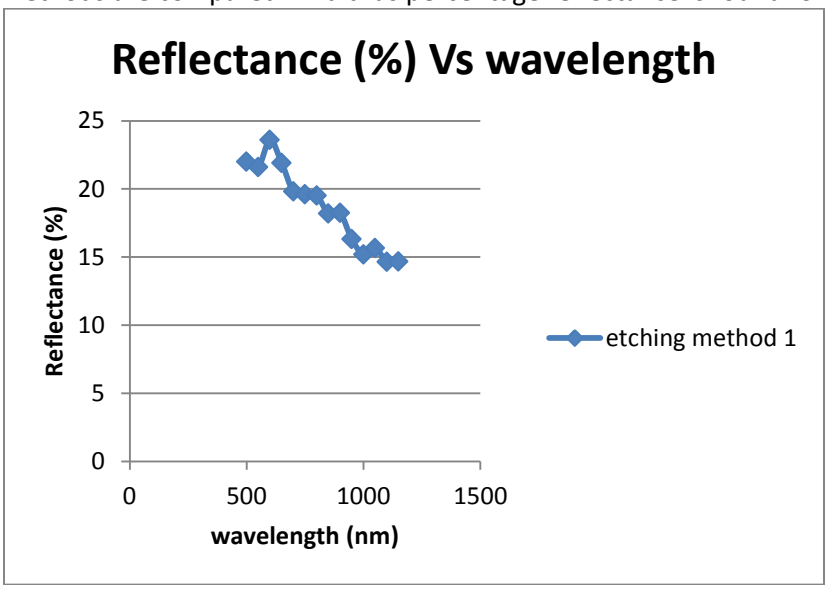


Figure5.12: (%) Reflectance graph of textured sample etched by recipe 1 with respect to mirror image

Lowest reflectance is approximately 14%. This line is normally a straight line and having approximate value of 12 to 18%. For etching method 1 the value of lowest reflectance lies within this limit.

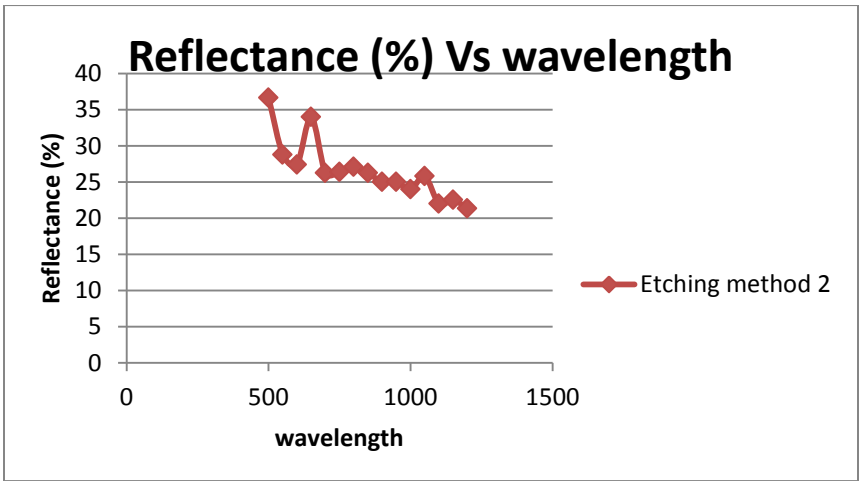


Figure 5.13.: (%) Reflectance graph of textured sample etched by recipe 2 with respect to mirror image

Lowest reflectance is approximately 21%. For etching method 2 the value of lowest reflectance lies near this limit.

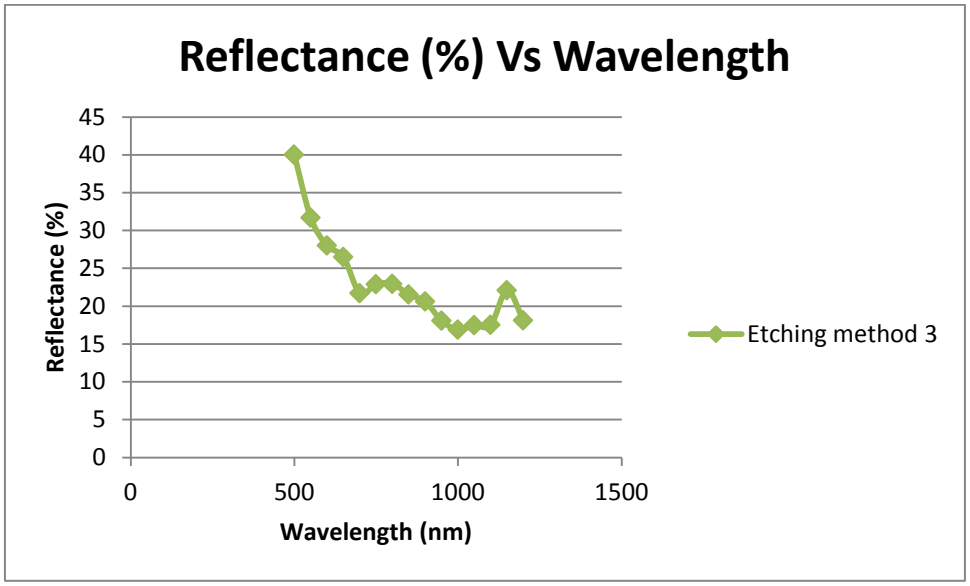


Figure 5.14: (%) Reflectance graph of textured sample etched by recipe 3 with respect to mirror image

Here Lowest reflectance is approximately 16.8%. For etching method 3 the value of lowest reflectance lies within this limit.

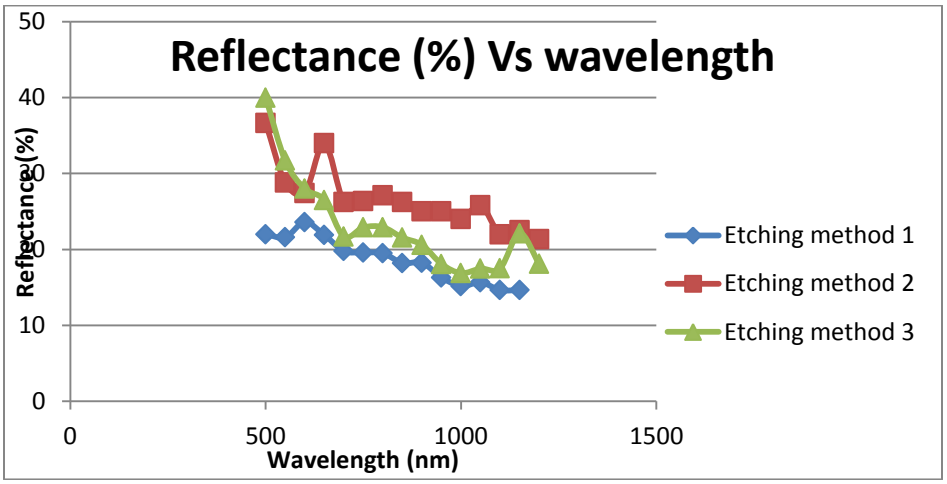


Figure5.15: (%) Reflectance graph of textured sample etched by recipe 1.2 and 3 with respect to mirror image

Figure shows the percentage of reflectance of textured wafer surface. From the graph it shows that only

14%, 21% and 17% light is reflected from the textured wafer surface etched by method 1, 2 and 3

respectively. That means the texturisation of wafer surface increase the light trapping capacity as well as the efficiency of a solar cell.

5.9. SEM image of textured Si wafer

SEM image was zoomed into ×5000, about 5µm across the whole field of view for image 1, 2 and 3.

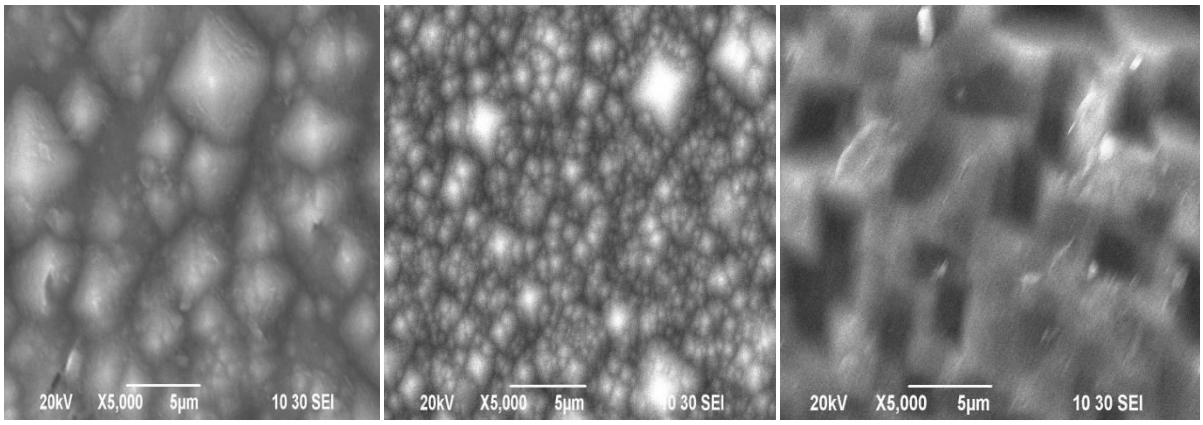


Figure 5.16: SEM image of textured Si wafers etched by recipe 1, 2 and 3 respectively

From the image it can be described that for sample Si wafer etched by method 1 bigger pyramids were found, though there were some blank spaces without pyramids. Bigger pyramid is a sign of homogenous texturing and uniformity of reflectance. Sample Si wafer etched by method 2 smaller pyramids were found and they were densely distributed. Si wafer etched by method 3 the SEM image was not clear to describe.

Chapter 6

Conclusion

6.1. Comparison of three etching recipes

While comparing three different saw damage removal methods recipe 1 showed bigger pyramid size (in SEM image) after texturing in compared with other two types etched samples. Big pyramids can be found by better etching method. From the SRM curve reduction of reflectance was observed for textured wafers etched by methods 1, 2 and 3, which is the main focus of texturing Si wafer. Percentage Reflectance for methanol/acetone recipe is 14%, while for hydrofluoric acid/ nitric acid is 17% and for Sodium Hydroxide/ hydrofluoric acid is 21%. The normal value of reduced reflectance is normally 12 to 18%. Here etching method 1 and 3 are acidic solution and method 2 is an alkali basic one.

6.2. Limitations

#Sharp SEM image is required for analyzing texturing effects. But the SEM image for etched by recipe 3 cannot be described because of lower image quality. Information like pyramid height, length between two pyramids and number of pyramids contain in cm^2 are essential. But we didn't have that information.

No mass change or brightness change was observed while etching with etching method 1, it seemed that it did not remove any saw damage.

6.3. Future scopes

By applying various cleaning conditions the effect of saw damage removal method on p-type Si wafer was observed. Result showed that with a better etching method percentage reflectance after texturing become lower. Pyramids with uniformity and homogeneity are required for getting higher cell efficiency. Methanol and acetone can be used for etching of Si wafers while preparing a complete cell in future in Solar Cell Fabrication & Research Division unit of Institute of Electronics of Bangladesh atomic energy commission instead of RCA cleaning steps (etching method 2 and 3). Methanol and acetone remove the organic compounds in SI wafers. The reflection is strongly reduced by the texturing process leading to improved external quantum efficiency. Further analysis with SEM effects of textured wafer by same etching methods can be made. Proper SEM image analysis would depict the better quality of this etching method.SRM image for raw, cleaned and textured surface can be compared with respect to mirror image, here we just compared the SRM image of mirror and textured surface of wafers

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