Department of Electrical and Electronic Engineering

Efficiency Improvement of Crystalline Silicon Solar Cell Using Different Texturing and ARC Methods in Bangladesh

A thesis submitted in fulfillment of the requirements for the award of the degree of Doctor of Philosophy in Electrical and Electronic Engineering

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Originality Statement

I hereby declare that this submission is the own work of **Mr. Galib Hashmi** and to the best of my knowledge it contains no materials previously published or written by another person, or substantial proportions of material which have been accepted for the award of any other degree or diploma at the University of Dhaka or any educational institution except where due acknowledgement is made in the thesis. Any contribution to the research by others, with whom **Mr. Galib Hashmi** has worked at University of Dhaka or elsewhere, is explicitly acknowledged in the thesis. I also declare that intellectual content of this is the product of **Mr. Galib Hashmi's** research work, except to the assistance from others is acknowledged.

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ABSTRACT

For the first time in 2015, monocrystalline silicon solar cell has been fabricated in one and only monocrystalline solar cell fabrication laboratory established in Atomic Energy Research Establishment (AERE), Savar, Bangladesh. The fabricated silicon solar cells in this laboratory have the efficiency of only 6.89% so far. The aim of this PhD research is to investigate the problems that result in the low efficiency and to find out the ways to improve the efficiency of solar cells with the available facilities in Bangladesh. It is very important to identify the problems of fabrication to enhance the efficiency. Through various experiment and minute observation of the cell fabrication process of AERE and the world standard process, the reasons of low efficiency have been determined. The reasons for achieving low efficiency: (i) are not having clean room class 100-1000, (ii) Czochralski (CZ) silicon wafer has been used instead of Float Zone (FZ) silicon wafer, usage of unknown edge isolation barrier paste, improper temperature at surface passivation technique, (iii) low shunt resistance, (iv) low minority carrier diffusion length (88 μm), (v) high series resistance (6.197 $\Omega.cm^2$), (vi) wafer bowing, (vii) unsmooth busbars and grid fingers, (viii) micro cracks, (ix) less aspect ratio, (x) not applying anti-reflection coating and (xi) lastly not utilizing oxygen and nitrogen gas in the metallization process.

Any change in the solar cell fabrication steps is too costly, wastage of resource material and the experimental procedure proves to be difficult and time consuming. For these reasons simulation has gained importance in the last few years. PC1D is a commercially available software most commonly used for solar cell modelling. Here simulation of monocrystalline silicon solar cell has been done using PC1D software. From the simulation it is seen that, the optimum value of *P*-type doping concentration is 1×10^{17} cm^{-3} and *N*-type doping concentration is 1×10^{18} cm^{-3}. Diffusion length of 200 μm gives optimum result. Both side textured wafer with pyramid height of 2-3 micrometer and equal angles of 54.74 degrees produces the best result in simulation.

Six different types of anti-reflection coating (ARC) layers have also been simulated using PC1D software. Result shows that the range of 500 nm – 700 nm would be suitable for designing an ARC. Single layer silicon nitride (Si_3N_4) ARC designed for 600 nm wavelength and with 74.257 nm thickness shows 20.35% efficiency. Significant increase in efficiency has been observed by applying ARC in respect to not applying any kind of ARC. After efficient solar cell modelling optimum efficiency of 20.67% is achieved by using SiO_2 surface passivation and Si_3N_4 ARC layer. The effects on voltage, current, photovoltaic efficiency, reflectivity and external quantum efficiency for various ARCs are also represented in this work.

Texturization is a very important aspect of solar cell fabrication process. Optimum texturization can increase the efficiency of solar cell. In this work practical experiments with different texturization process have been done. Different concentrations of Na_2CO_3 - $NaHCO_3$ solution, KOH-IPA solution and TMAH solution with different time intervals have been investigated for texturization process. Furthermore, saw damage removal process has been conducted with 10% NaOH solution, 20 wt% KOH - 13.33 wt% IPA solution and HF/Nitric/Acetic Acid (HNA) solution.

The surface morphology of saw damage, saw damage removed surface and textured wafer have been observed using optical microscope and Field Emission Scanning Electron Microscopy (FE-SEM). Texturization causes pyramidal micro structures on the surface of (100) oriented monocrystalline silicon wafer. The height of the pyramid on the silicon surface varies from 1.5 µm to 3.2 µm and the inclined planes of the pyramids form acute angles. Contact angle value indicates that the textured wafers surface fall in between near-hydrophobic to hydrophobic range. Less than 0.1% reflectance has been achieved when textured with 0.76 wt% KOH - 4 wt% IPA solution for 20 minutes. Furthermore, an alternative route of using 1 wt% Na_2CO_3 - 0.2 wt% $NaHCO_3$ solution for 50 min has been exploited in the texturization process.

N-Type layer (Emitter) has been formed by diffusion process over an as-cut monocrystalline *P*-type silicon wafer (Base). The diffusion process has been carried out at 875 °C in an Atmospheric Pressure Chemical Vapor Deposition (APCVD) chamber. In the APCVD chamber $POCl_3$ (Phosphorus Oxychloride), N_2 and O_2 gas has been used. For the diffusion process, the deposition time and drive time variations are 5, 10, 15, 20, 30 min and 10, 15, 20, 25 and 35 min, respectively. After diffusion process hot point probe experiment has been carried out and it ensures that *N*-Type layer has been formed. Experimentally obtained values of the emitter sheet resistance are 65.25 Ω/□, 44.62 Ω/□, 13.53 Ω/□, 32.75 Ω/□ and 55.38 Ω/□. From the sheet resistance values, electron concentration has been theoretically calculated. From sheet resistance values and considering low manufacturing cost, 5 min diffusion and 10 min drive time provides the suitable recipe to create a *N*-type layer upon *P*-type silicon substrate.

Apart from fabrication of solar cell, characterizations of different silicon wafer and solar cell have been done. The characterizations are: (i) surface morphology determination using optical microscope and SEM, (ii) surface roughness and height determination using Surface Profilometer, (iii) band gap measurement using Spectral Response Measurement Machine, (iv) fill factor and efficiency measurement using LIV tester, (v) series and shunt resistance measurement, (vi) sheet resistance determination using Four Point Probe System, (vii) *P*-type and *N*-type determination using Hot Probe Method, (viii) thickness measurement of different wafers using Dial Indicator, (ix) reflectance measurement different wafers using UV-VIS-NIR Spectroscopy, (x) busbars and grid fingers height, width and aspect ratio measurement and (xi) EDS measurement of different doped wafer. All the characterization processes and results are discussed in details in this dissertation. Lastly, limitation and remedies of fabrication of solar cell in Bangladesh has been discussed in this thesis.

Publication List

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[2] **Galib Hashmi**, Abdur Rafiq Akand, Mahbubul Hoq and Habibur Rahman, "**Study of the Enhancement of the Efficiency of the Monocrystalline Silicon Solar Cell by Optimizing Effective Parameters Using PC1D Simulation**", Silicon, **Springer**, Netherlands, Volume 10, Issue 4, pp. 1653-1660, 2018, Print ISSN: 1876-990X, Online ISSN: 1876-9918.
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[3] **Galib Hashmi**, Muhammad Junaebur Rashid, Zahid Hasan Mahmood, Mahbubul Hoq and Md. Habibur Rahman, "**Investigation of the impact of different ARC layers using PC1D simulation: application to crystalline silicon solar cells**", Journal of Theoretical and Applied Physics, Volume 12, Issue 4, pp. 327–334, ISSN 2251-7227, **Springer**, December 2018.
DOI 10.1007/s40094-018-0313-0

[4] **Galib Hashmi**, Md. Abdur Rafiq Akand, Mohammad Khairul Basher, Mahbubul Hoq and Md. Habibur Rahman, **"Fabrication of Crystalline Silicon Solar Cell in Bangladesh: Limitations and Remedies"**, International Journal of Scientific & Engineering Research, pp. 581-586,Volume 7, Issue 5, May -2016. ISSN: 2229-5518 (U.S.A)
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[6] **Galib Hashmi**, Muhammad Hasanuzzaman, Mahbubul Hoq and Md. Habibur Rahman, "**Optimization of Surface Reflectance of *P*-type Mono-Crystalline Silicon Wafer using Na_2CO_3-$NaHCO_3$ Solution",**
Bangladesh Journal of Physics (BJP), pp. 27-34, Volume 21, Issue 1, June 2017. ISSN: 1816-1081.

[7] **Galib Hashmi**, Md. Shahriar Basher, Mahbubul Hoq and Habibur Rahman, "**Problem Analysis of Fabricated Monocrystalline Silicon Solar cell in Bangladesh**", Dhaka University Journal of Applied Science & Engineering (DUJASE), Volume 4, No. 1, pp. 27-33, 2017, Print ISSN: 2218-7413.
http://journal.library.du.ac.bd/index.php?journal=DUJAPSE&page=issue&op=view&path%5B%5D=139

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[2] **Galib Hashmi**, Mahbubul Hoq, Md. Habibur Rahman and Shahida Rafique, **"Proposed Technique to Improve Efficiency of Crystalline Silicon Solar Cell"**, National Seminar and Exhibition on Renewable Energy 2016 on 27th January at Mokarram Bhaban, Physics Auditorium DU.

[3] **Galib Hashmi**, Mohammad Khairul Basher, Mahbubul Hoq and Md. Habibur Rahman, **"Band Gap Measurement of *P*-Type Monocrystalline Silicon Wafer Using Spectral Response Measurement System"**, National Conference on Physics-2017, (Bangladesh Physical Society), 5th January, 2017, at Bangladesh Atomic Energy Commission, Dhaka University Campus.

[4] M. Asrafusjaman, **Galib Hashmi**, T. Akter, M. A. R. Akand, M. K. Basher and K. Uddin, **"Comparative Study on the Surface Texturing Method for Crystalline Silicon Solar Cell"**, National Conference on Physics-2017, (Bangladesh Physical Society), 6th January, 2017, at Bangladesh Atomic Energy Commission, Dhaka University Campus.

[5] **Galib Hashmi**, Muhammad Hasanuzzaman, Mahbubul Hoq and Md. Habibur Rahman, "**Optimization of Surface Reflectance by Formation of Pyramidal Microstructure on *P*-type Mono-Crystalline Silicon Substrate Using KOH –IPA Solution**", National Renewable Energy and Green Expo, March, 2017, DU.

[6] **Galib Hashmi**, Mohammad Junaebur Rashid, Zahid Hasan Mahmood, Mahbubul Hoq and Md. Habibur Rahman, "**Performance Study of Single Layer TiO_2/Si_3N_4 Anti-reflecting Coating for Silicon Solar Cell Using Simulation Software**", 18th National Renewable Energy Conference & Green Expo-2018. Presented February 13, 2018 at Senate Bhavan Seminar Room, DU.

[7] S. Biswas, M. K. Basher, M. R. Ahmed, **G. Hashmi**, S. Huque "**Study and Analysis of Doping Concentration of Monocrystalline Silicon Solar Cells Using Hall Effect Measurement System**" International Conference on Physics,- 2018. Held at 8th March at Mokarram Bhaban, DU.

[8] M. R. Ahmed, M. K. Basher, S. Biswas, **G. Hashmi**, S. Huque "**Study and Analysis the Effect of Doping Time on the Sheet Resistance Monocrystalline Silicon Solar Cell**" International Conference on Physics-2018. Held at 8th March at Mokarram Bhaban, DU.

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Table of Contents

Page No.

Page No.

Page No.

Page No.

List of Figures

Figures — Page No.

Figures Page No.

Figures Page No.

List of Tables

Tables Page No.

Chapter 1

INTRODUCTION

1.1 Introduction

In Bangladesh, Electric power consumption in 2011 was 39.53 billion kWh [1], whereas in 2015 it was 48.98 billion kWh [2]. Statistics shows that the demand for energy is increasing not only in Bangladesh but all over the world. Each country is making their own necessary steps to encounter this problem. However, the major problem lies in the fact that fossil fuel will not last forever. Also, oil is not found everywhere, coal is still abundant and cheap but polluting, natural gas is scarce and nuclear energy production is costly and risky. Since that oil, coal, gas, nuclear power is not green energy, not abundant and will not last forever the only option is to turn to renewable energy. Scientists and researchers predicts that within 2050 it is possible to achieve 100% renewable energy in 139 countries if proper policies and steps are taken [3].

In agreement with the scientists, the whole world is making necessary steps to achieve renewable energy as much as possible. The Renewable Energy Policy of Bangladesh envisions that 10% of total energy production will be achieved by renewable energy within 2020 [4]. Furthermore, on 22nd April, 2016 Bangladesh signed the Paris Agreement [5]. The main goal of Paris Agreement is to reduce greenhouse gas emission and keeping global warming well below 2° Celsius and ensuring planetary habitability for today and for future generation.

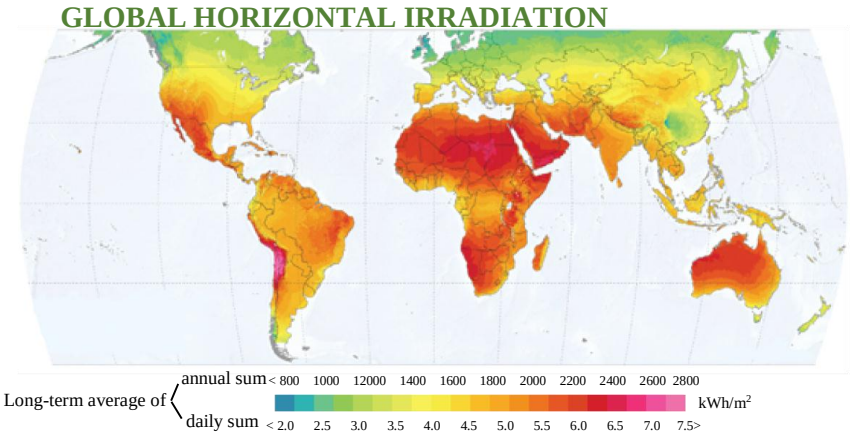

Figure 1.1 Global Solar Irradiation: Photo Courtesy of Solargis [6]

Taking all these things in consideration, Bangladesh Government is currently giving emphasis on generating electricity from renewable energy sectors. Currently (Up to March, 2018) the electricity generation percentage from renewable energy is 3.10%. Among all the renewable energies (biogas, biomass, wind, solar, hydro) in Bangladesh, 53.74% electricity is generated from solar photovoltaic technology [7]. This is because tropic of cancer passes through Bangladesh and thus the daily solar irradiation intensity is good (Figure 1) and varies from 3 to 6.5kW/m^2 per day [8]. Also by considering the technical, environmental and economic aspect - solar photovoltaics [9] is the best option for utilizing renewable energy and to eradicate the energy crisis in a land shortages country like Bangladesh.

Considering these advantages, already more than 4.5 million solar home systems (SHSs), 3 solar mini grids and about 671 solar irrigation systems have been established in Bangladesh. Initiatives have been taken to install 3 Mega Watt of solar rooftop system in different locations. In a solar radiation abundant country like Bangladesh [10], solar PV plant has the extensive potentiality to eradicate the electricity crisis and can also play a major role towards achieving 100% renewable energy.

Though there is a vast demand of solar panels now and in the future, in this country most of the solar panels are mainly imported from abroad. Few local companies like Rahimafrooz Renewable Energy Ltd, Electro Solar Power Ltd. etc are making solar panels in Bangladesh. But unfortunately the main component of solar panel which is solar cell is imported from abroad. Thus to reduce the import of solar cells and solar panels from abroad and to create more employment opportunity, local fabrication of solar cell is very much necessary and is the demand of the days.

To fulfill this dream, for the first time in 2015, monocrystalline silicon solar cell has been fabricated at one and only monocrystalline solar cell fabrication laboratory established in Atomic Energy Research Establishment (AERE), Savar, Bangladesh. However, the fabricated silicon solar cells in this laboratory yielded efficiency of only 6.89% so far [11]. Improvement of efficiency is in dire need to compete with commercially available solar cell.

Thus the main goal of this research is to fabricate efficient solar cell in Bangladesh. To do that the problems that cause low efficiency have been investigated first in this research work, because it is very important to identify the problems of fabrication to enhance the efficiency. It is expected that after finding the problems, appropriate measures can be adopted to improve the efficiency of solar cell.

A lot of limitations have been found in the existing fabrication procedure in AERE. One of the problems are not having a clean room. Secondly, low shunt resistance (234 ohm) and high series resistance (6.197 $\Omega.cm^2$) is observed in the locally fabricated solar cell. During fabrication low quality CZ (Czochralski) wafer has been used. Major flaw has been observed during edge isolation and anti-reflection coating (ARC) process. Minority carrier diffusion length (88 μm) has been found low. Furthermore, problems like wafer bowing has been observed and the peak height of wafer bowing has been measured. Straightness of the busbars and grid fingers have been analyzed, results are found not satisfactory. Optical microscopic analysis shows micro cracks in busbars. Dektak 150 Surface Profiling System has been used to measure surface roughness of grid fingers of overseas and solar cells fabricated in Bangladesh. The result shows more unevenness in grid fingers of locally fabricated solar cells. Also, no oxygen and nitrogen gas is used in the metallization process during fabrication, as RTA (Rapid Thermal Annealing) Furnace does not have the option of providing oxygen and nitrogen gas. All these problems and remedies are elaborately discussed in this PhD thesis.

It is well known that, to introduce any change in the solar cell fabrication process is too expensive and the experimental procedure proves to be difficult. As change in any aspect of fabrication process is a difficult task, simulation has gained importance over the past few years. PC1D is a commercially available software most commonly used for solar cell modelling and simulation. Here, simulation of monocrystalline silicon solar cell has been done using PC1D software. Impacts of different solar cell parameters, with their effects on power and efficiency

has been investigated. The simulation also gives insight about the range and impact of doping concentration, diffusion length, texturing and anti-reflection coating.

Anti-reflection coating (ARC) is not applied in the locally fabricated solar cell because of having no equipment related to ARC. Hence, this research work conducted the simulation of different types of ARC. Simulation has been done to find out the suitable ARC for crystalline silicon solar cell. In this research, the impact without ARC and with six types of ARC such as Titanium dioxide (TiO_2), Zinc oxide (ZnO), Zinc sulfide (ZnS), Silicon dioxide (SiO_2), Silicon nitride (Si_3N_4) and Silicon carbide (SiC) have been investigated separately for crystalline silicon solar cell. Furthermore, simulations ranging from 250 nm to 1200 nm wavelengths have been conducted to find out the most suitable wavelength required for designing ARC in solar cell. Surface passivation upon ARC has been applied and its impact has been investigated. The ARC simulation also gives insight about its effects on efficiency of solar cell. Moreover, the reflectivity for the wavelength range of 250 nm to 1250 nm of all the ARCs and external quantum efficiency has also been thoroughly discussed in this PhD thesis.

Texturization on the monocrystalline silicon substrate reduces reflection and enhances light absorption of the substrate. Thus texturization is one of the key methods to increase the efficiency of solar cell. Considering as-cut monocrystalline silicon wafer as base substrate, in this work different concentrations of Na_2CO_3 and $NaHCO_3$ solution, KOH-IPA (Isopropyl Alcohol) solution and Tetramethylammonium Hydroxide (TMAH) solution with different time intervals have been investigated for texturization process. Since there are lots of texturization recipes, one of the goal of this research work is to find a suitable texturization recipe and optimize the recipe based on timing, concentration and temperature. Furthermore, to see the impact of saw damage removal process, the saw damage removal process has been applied with 10% NaOH solution, 20 wt% KOH-13.33 wt% IPA solution and HF/Nitric/Acetic Acid (HNA) solution. The surface morphology of as-cut wafer with saw damage, saw damage removed surface and textured wafer are observed using optical microscope and field emission scanning electron microscopy (FE-SEM). Texturization causes pyramidal micro structures on the surface of (100) oriented monocrystalline silicon wafer. The height and angle of the pyramid on the silicon surface have been measured. Contact angle has also been determined to find out whether the textured wafer's surface is hydrophobic or not. Moreover, in this work different characterization process has been done to find out different parameters of the locally fabricated solar cell. Finally solar cell has been fabricated with the available equipment and the whole process with limitations and remedies has been elaborated in this PhD thesis [8, 11].

1.2 Research Objectives

The efficiency of the locally fabricated crystalline silicon solar cell is only 6.89%, thus efficiency improvement is necessary. Therefore, the aim of this research is to improve the efficiency of crystalline silicon solar cells. In general, solar cell efficiency can be improved by different texturization process and applying anti-reflection coating (ARC). That is why in the PhD thesis title, different texturing and ARC methods in Bangladesh has been included. So, the full title of the PhD thesis has been selected as "Efficiency Improvement of Crystalline Silicon Solar Cell Using Different Texturing and ARC Methods in Bangladesh".
Objectives provide an accurate description of the specific planning, strategies and actions which is needed in order to reach the goal of the thesis work. The objectives of the thesis are mentioned below:

- To find out the problems of locally fabricated solar cells that result in low efficiency solar cell
- Simulation of solar cell using PC1D software
- Simulation of different anti-reflection coating upon solar cell using PC1D software
- Different type of texturization and saw damage removal process using wet chemicals and to find out the optimum recipe
- Use of $POCl_3$ deposition technique and to find out the optimum diffusion recipe using
- Different characterization of solar cell
- Developing an efficient solar cell

1.3 Review of Literature

The development of the solar cell originate from the work of the French experimental physicist Antoine-César Becquerel back in the 19th century. In 1839, Becquerel discovered (although he could not fully explain) the photovoltaic effect while experimenting with an electrolytic cell containing two metal electrodes. He found that certain metals and solutions would produce small amounts of electric current when exposed to light.

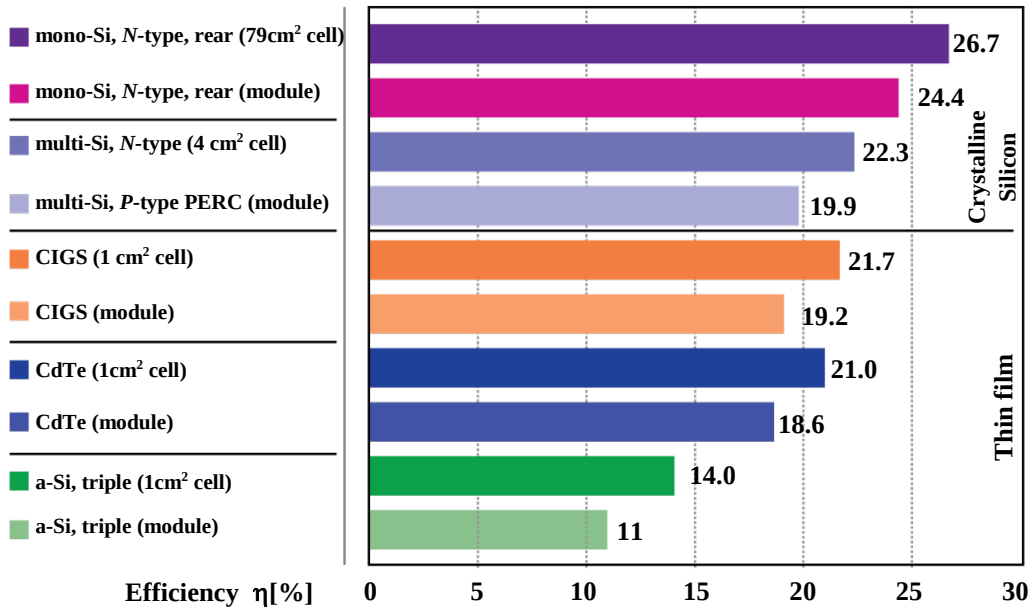

Figure 1.2 Efficiency Comparison of Solar Cell Technologies: Photo Courtesy of Fraunhofer Institute for Solar Energy Systems ISE [12]

Technology of solar cell has progressed a lot since then. In 1954, three other American researchers, G.L. Pearson, Daryl Chapin, and Calvin Fuller, demonstrated a further-refined silicon solar cell capable of a 6% energy conversion efficiency (in direct sunlight). In 1985, The University of South Wales breaks the 20% efficiency barrier for silicon solar cells under one sun conditions. Currently there are several solar cell technologies available in the market. Crystalline silicon solar cell leading the market with 94% of the total production by 2016 [13]. Whereas in 2016, the market share of all thin film technologies amounted to about 6% of the total annual production. This is because crystalline silicon solar cells efficiency is still better than thin film solar cell. By looking the solar cell efficiency table (version 51, year 2017), [14], it is seen that monocrystalline silicon solar cell has the highest efficiency of 26.7 %. Whereas

highest efficiency of thin film solar cell is 21.7% as shown in Figure 2. This efficiency is achieved by Copper Indium Gallium Selenide (CIGS) thin film solar cell. As monocrystalline silicon solar cell still has the highest efficiency, back in the year 2014 the one and only monocrystalline silicon solar cell fabrication laboratory has been established in Atomic Energy Research Establishment (AERE), Savar, Bangladesh Atomic Energy Commission (BAEC). With the help of Malaysian scientists the first silicon solar cell has been fabricated in this laboratory and the efficiency of that solar cell was 0.8 %. Then research work was continued to improve the efficiency of solar cell. In 2015, a solar cell has been fabricated with 6.89% efficiency. That is the highest efficiency achieved so far in Bangladesh. It's still a long way to go in fabricating high efficiency solar cell in Bangladesh. The BAEC scientists, MSc. and PhD students of different universities are trying to improve the efficiency of solar cell. However, more research work regarding this issue needs to be carried out to fabricate high efficient solar cell in Bangladesh. So far in the Department of Electrical and Electronic Engineering, University of Dhaka one PhD work has been completed on locally fabricated solar cell. It is done by Dr. Nahid Akter (Registration & Session No. 138/2011-2012) and the title of the thesis is "Study on Structural, Optical and Electrical Properties of Single Junction Mono-crystalline Silicon Solar Cells" [15]. From the title it is clearly understand that the main emphasis of the work is characterization of solar cell. Characterization has been done using four point probe, Energy-dispersive X-ray spectroscopy (EDS), reflectivity measurement, surface profilometer and SEM analysis on raw, textured and diffused wafer. In this thesis, all these characterization has been done with more details and elaboration. For example, only one measurement of four point probe has been taken by Dr. Nahid Akter. But only one measurement cannot give the accurate result so several measurements on several samples has been done in this present work. In the previous PhD thesis relative reflectivity measurement has been done. For this reason in this present work more accurate measurement that is absolute reflectivity measurement on different sample has been conducted. More accurate measurement using SEM, surface profilometer and EDS have been also taken and deeply elaborated in this PhD thesis.

Study reveals that Dr. Nahid Akter's main work is concentrated especially on hot-point probe technique. Details of that process is elaborated in that thesis. However, here hot point probe technique has been conducted with a different technique and not elaborated as Dr. Nahid Akter as it is discussed in her thesis. Furthermore, Dr. Nahid Akter worked in the Thin Film Laboratory and Advanced Solar Cell Fabrication Laboratory, Solar Energy Research Institute (SERI), Universiti Kebangsaan Malaysia. Where she formed *N*-type layer upon *P*-type material using P_5O_9 solution. This work has not been done and hence not discussed in any section of this thesis. Lastly, she fabricated a solar cell with 5.96% efficiency and currently the efficiency of solar cell is 6.89%. So the main work conducted in this thesis are problem analysis of the locally fabricated solar cell, remedies, simulation of solar cell, simulation of anti-reflection coating, texturization process, diffusion process and fabrication process. All the process is discussed in details in this thesis. Literature review of texturization and simulation of anti-reflection coating has been separately discussed in Chapter 9, section 9.1 and Chapter 7, section 7.1 respectively of this PhD dissertation [16-17]. Furthermore, detailed characterization (Absolute Reflectance, Series and Shunt Resistance, Four Point Probe Measurement, Energy Dispersive Spectroscopy (EDS), Optical Microscopy etc.) which is not done before has also been done here. Thus, it can be said that this thesis is completely different from Dr. Nahid Akter PhD thesis.

1.4 Thesis Paper Outline

This thesis report has been completed in twelve chapters:

Chapter 1: An introduction of the PhD research work. Some recent works related to this thesis are described.

Chapter 2: In the 2nd chapter, description of the theories related to this work are given in details.

Chapter 3: Mainly focused on the characterization and fabrication equipment which are used in this study.

Chapter 4: In this chapter, the fabrication of solar cell in Bangladesh has been discussed.

Chapter 5: Problem analysis of the locally fabricated solar cell has been discussed in this chapter.

Chapter 6: Simulation of solar cell has been done using PC1D software. The whole simulation process is elaborated in this chapter.

Chapter 7: Simulation of six different types of anti-reflection coatings and their effects have been explained.

Chapter 8: Determination of band gap using spectral response measurement system has been discussed.

Chapter 9: Description of texturization and saw damage removal process of different silicon wafer has been given in this chapter.

Chapter 10: This chapter discusses about the of *N*-type layer diffusion process.

Chapter 11: Characterization of solar cell and different silicon wafer is briefly discussed here.

Chapter 12: This chapter gives the fabrication of solar cell and the conclusion of this PhD research work.

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Chapter 2

THEORETICAL BACKGROUND OF THE STUDY

2.1 Introduction

Theories are formulated to explain, predict, and understand phenomena of existing knowledge. In many cases, theory helps one to challenge and extend prevailing knowledge. In this chapter, the theories which are the prerequisite to the PhD thesis are briefly elaborated. Specifically, theories extensively related to solar cell are discussed here.

2.2 Solar Cell

A solar cell (also called a photovoltaic cell, as shown in Figure 1) is an electrical device that converts the energy of light directly into electricity by the photovoltaic effect [1]. Where, the photovoltaic effect is the process that generates voltage in a photovoltaic cell when it is exposed to light or other radiant energy [2]. To understand the photovoltaic effect and solar cell some basic theory about semiconductors as well as information on *P-N* junctions is to know first. So, these topics are explained first in the following sections.

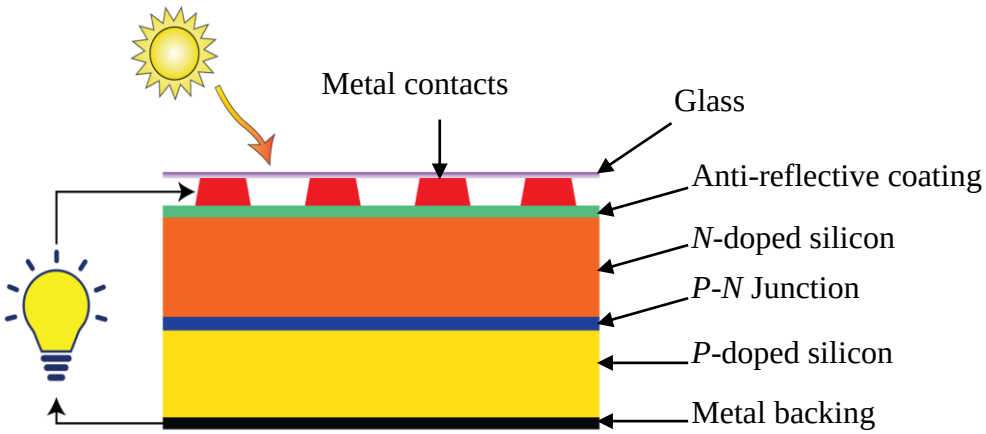


Figure 2.1 Basic structure of a silicon solar cell

2.2.1 Band Theory: Conductor, Semiconductor and Insulator

In an atom, electrons revolve in the orbits around the nucleus. The electrons are revolving in different orbits. Some orbits are closer to the nucleus and some are away from the nucleus. The electrons closer to the nucleus possess lower energy than those farther from nucleus. In atom, if the distance between electrons and nucleus increases, the potential energy of the electrons is increased. Thus, it can be said that the position occupied by an electron in an atom signifies a certain energy level of that electron.

When a number of atoms are brought together, the electrons of one atom experience forces of other atoms. This effect is most prominent in the outer most orbits. Due to this force, the energy levels, which are sharply defined in an isolated atom, are now broadened into energy bands. Due to this phenomenon generally two bands result, namely valance band and conduction band.

Valance band is defined as the outermost orbital of an atom, where electrons are bounded to the nucleus and cannot be removed as free electron. Whereas the conduction band is the highest energy level or orbital in outer most shell, in which electrons are free enough to move. Furthermore there is an energy gap that separates the valance band and conduction band. This gap is called forbidden energy gap or band gap (Eg).

According to band gap materials can be classified to three types. They are conductor, insulator and semiconductor as shown in Figure 2.2.

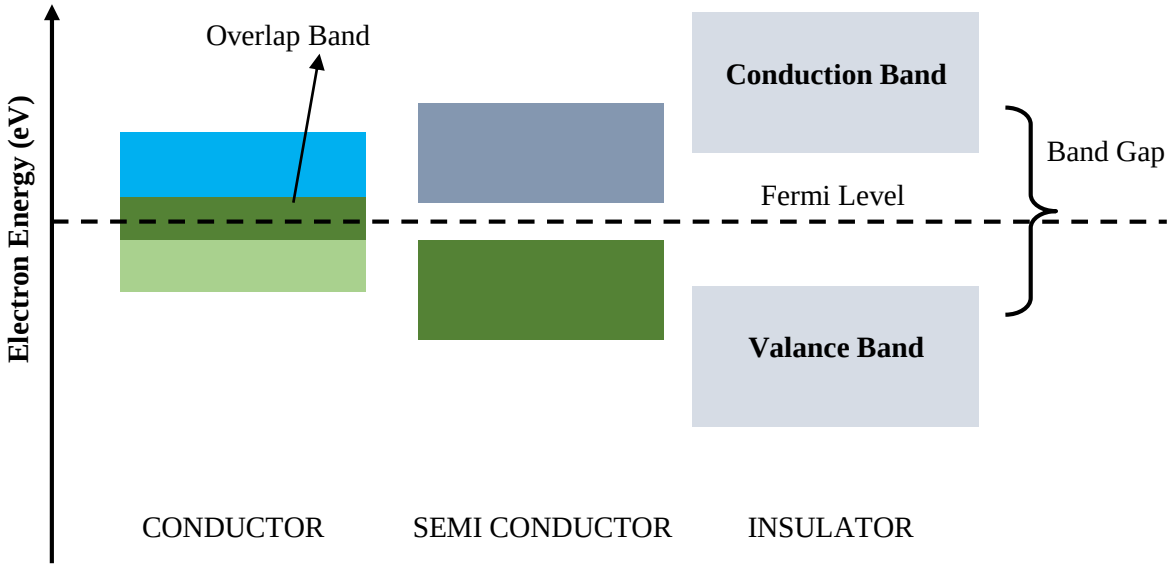


Figure 2.2 Conductor, Insulator and Semiconductor [4]

In a conductor, the valance band and conduction band are very closer to each other and may even overlap. Thus, by receiving a very small amount of energy from external heat or electrical energy source, the electrons readily ascend to conduction band from valance band. Such electrons are known as free electrons. These free electrons are responsible for current, that flows through a conductor. When external electric source is connected to a piece of metal, the free electrons start flowing towards higher potential terminal of the source, causing current to flow in the conductor. An example of conductor is metal.

The opposite of the conductor is an insulator. The electrical conductivity of an insulator is nil. In insulator the band gap is very large and as a result the energy required by the electron in the valance band to cross over to the conduction band is practically large. Thus insulators do not conduct electricity easily. An example of insulator is wood.

In semiconductor the valance band and conduction band are separated by a forbidden gap (band gap less than 5 eV). At low temperature, no electron possesses sufficient energy to occupy the conduction band and thus no movement of charge is possible. But at room temperature it is possible for some electrons to gain sufficient energy and make transitions in conduction band. The density of electrons in conduction band at room temperature is not as high as in metals,

thus cannot conduct electrical current as good as metal. The electrical conductivity of semiconductor is not as high as metal but also not as poor as electrical insulator. That is why, this type of material is called semiconductor. In solid state physics, this level, where the probability to find an occupied state is known as the Fermi level and it lies exactly between the conduction and the valence band.

Most of electronics are made of semiconductor materials. Especially a large number of solar cells are made of semiconductor. Thus vast knowledge of semiconductor is necessary in fabricating solar cell. Some important information about semiconductor is discussed in the following section.

2.2.2 Intrinsic and Extrinsic Semiconductors

In most pure semiconductors at room temperature, the population of thermally excited charge carriers is very small. For example, the number of thermally excited electrons cm^{-3} in silicon (Si) at 298 K is 1.5×10^{10}. In gallium arsenide (GaAs) the population is only 1.1×10^{6} electrons cm^{-3}.

Given these numbers of charge carriers, it is not surprising that, when they are extremely pure, silicon and other semiconductors have high electrical resistivity, and therefore low electrical conductivity. This problem can be overcome by doping a semiconducting material with impurity atoms. Even very small controlled additions of impurity atoms at the 0.0001% level can make very large differences in the conductivity of a semiconductor.

It is easier to begin with a specific example. Silicon is a group IV element, and has four valence electrons per atom. In pure silicon, the valence band is completely filled at absolute zero. At finite temperature the only charge carriers are the electrons in the conduction band and the holes in the valence band that arise to the conduction band as a result of the thermal excitation of electrons. These charge carriers are called intrinsic charge carriers, and necessarily there are equal numbers of electrons and holes. Pure silicon is, therefore, an example of an intrinsic semiconductor.

If a very small number of atoms of group V element such as phosphorus (P) are added to the silicon as substitutional atoms in the lattice, additional valence electrons are introduced into the material because each phosphorus atom has five valence electrons. These additional electrons are bound only weakly to their parent impurity atoms (the bonding energies are of the order of hundredths of an eV), and even at very low temperatures these electrons can be promoted into the conduction band of the semiconductor. This is often represented schematically in band diagrams by the addition of 'donor levels' just below the bottom of the conduction band, as in the Figure 2.3.

The presence of the dotted line in this schematic does not mean that there now exist allowed energy states within the band gap [5]. The dotted line represents the existence of additional electrons which may be easily excited into the conduction band. Semiconductors that have been doped in this way will have a surplus of electrons, and are called *N*-type semiconductors. In such semiconductors, electrons are the majority carriers. Conversely, if a group III element, such as aluminium (Al) / boron (B), is used to substitute for some of the atoms in silicon, there will be a deficit in the number of valence electrons in the material. This introduces electro*N*-accepting levels just above the top of the valence band, and causes more holes to be introduced

into the valence band. Hence, the majority charge carriers are positive holes in this case. Semiconductors doped in this way are called *P*-type semiconductors (Figure 2.4).

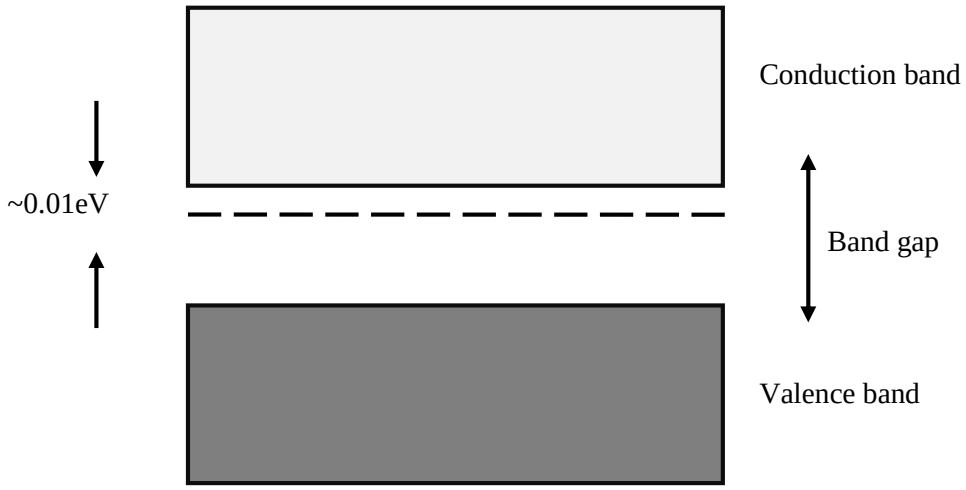


Figure 2.3 *N*-type Semiconductor

Figure 2.4 *P*-type Semiconductor

Doped semiconductors (either *N*-type or *P*-type) are known as extrinsic semiconductors. It should be remembered that in an extrinsic semiconductor there is a contribution to the total number of charge carriers from thermally generated intrinsic electrons and holes, but at room temperature this contribution is often very small in comparison with the number of charge carriers introduced by the controlled impurity doping of the semiconductor.

2.2.3 *P*-*N* Junction

The *P*-type semiconductor is electrically neutral but it has positive holes (lack of electrons) in its structure, which can accommodate excess electrons. Similarly the *N*-type semiconductor is electrically neutral but has excess electrons, which are available for conduction. Both types of semiconductors are placed side by side and shown in Figure 2.5.

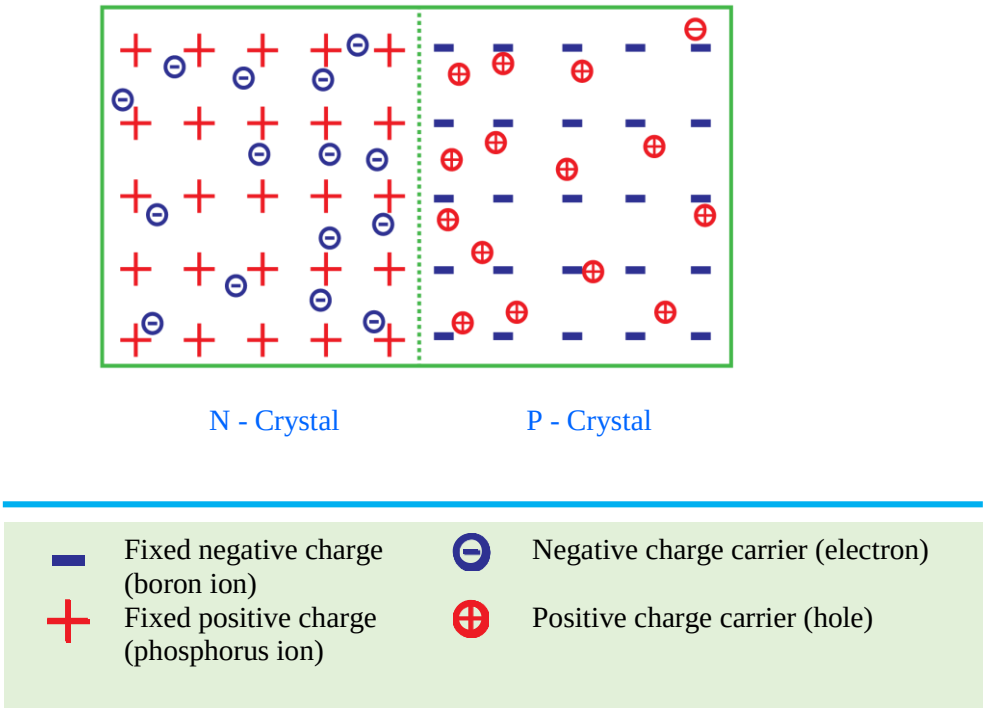


Figure 2.5 *P*-type and *N*-type Semiconductor Placed Side by Side

Now, by joining *P*-type and *N*-type semiconductor materials *P*-*N* junctions are formed [6]. Since the *N*-type region has a high electron concentration and the *P*-type a high hole concentration, electrons diffuse from the *N*-type side to the *P*-type side. Similarly, holes flow by diffusion from the *P*-type side to the *N*-type side as shown in Figure 2.6.

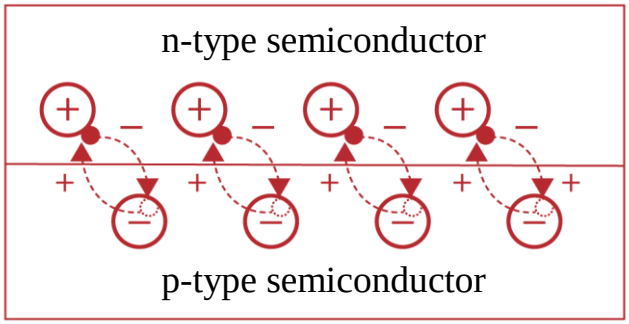


Figure 2.6 Diffusion Process

If the diffusion of electrons and holes are not obstacle, this diffusion process would continue until the concentration of electrons and holes on the two sides are the same, as happens if two gasses come into contact with each other.

However, in a *P*-*N* junction, when the electrons and holes move to the other side of the junction, they leave behind exposed charges on dopant atom sites, which are fixed in the crystal lattice and are unable to move. On the *N*-type side, positive ion cores (donor) are exposed. On the *P*-type side, negative ion cores (acceptor) are exposed as shown in Figure 2.7.

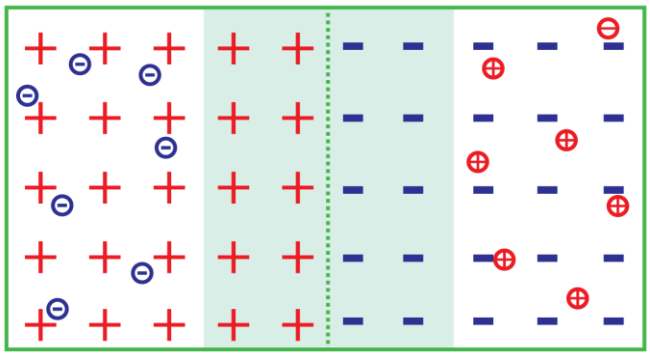


Figure 2.7 Positive and Negative Exposed ions in *P*-type and *N*-type Semiconductor

An electric field Ê forms between the positive ion cores in the *N*-type material and negative ion cores in the *P*-type material. This region is called the depletion region [7] (Figure 2.8). Since the electric field quickly sweeps free carriers out, hence the region is depleted of free carriers.

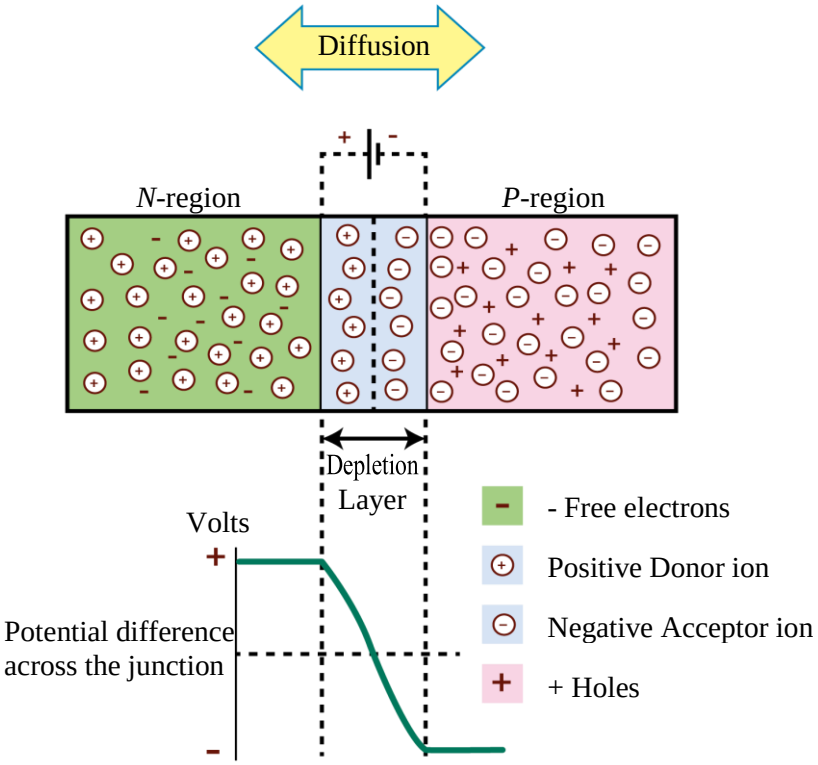


Figure 2.8 Depletion Layer

Thus a "built in" potential is formed at the junction. Because in the presence of impurity ions on both sides of the junction establish a barrier voltage across this region with the *N*-side at a positive voltage relative to the *P*-side. The problem now is that a free charge requires some extra energy to overcome the barrier that now exists for it to be able to cross the depletion region junction.

This electric field created by the diffusion process has created a " in-built potential difference" across the junction with an open-circuit (zero bias) potential of:

$$E_0 = V_T \ln \left(\frac{N_D N_A}{n_i^2}\right) \text{ ……..(1) [8]}$$

Where, E_0 is the zero bias junction voltage, V_T is the thermal voltage of 26 mV at room temperature, N_D and N_A are the impurity concentrations and n_i is the intrinsic concentration.

A suitable positive voltage (forward bias) applied between the two ends of the *P-N* junction can supply the free electrons and holes with the extra energy. The external voltage required to overcome this potential barrier that now exists is very much dependent upon the type of semiconductor material used and its actual temperature.

Typically at room temperature the barrier voltage across the depletion layer for silicon is about 0.6 – 0.7 volts and for germanium is about 0.3 – 0.35 volts. This potential barrier will always exist even if the device is not connected to any external power source, as seen in diodes.

The significance of this in-built potential across the junction, is that it opposes both the flow of holes and electrons across the junction and is why it is called the potential barrier. In practice, a PN junction is formed within a single crystal of material rather than just simply joining or fusing together two separate pieces.

2.3 Principles of Solar Cell Operation

As stated earlier solar cell converts light energy into the electrical energy. This is because a solar cell is basically a *P-N* junction diode. It utilizes photovoltaic effect to convert light energy into electrical energy.

Although this is basically a junction diode, but constructionally it is little bit different form conventional *P-N* junction diode [9]. Here a very thin layer of *N*-type semiconductor is grown on a relatively thicker *P*-type semiconductor. There are few finer electrodes (called busbars and grid fingers) are on top of the *N*-type semiconductor layer. Just below the *P*-type layer there is a *P-N* junction. Furthermore, there is also an electrode at the bottom of the *P*-type layer known as the back contact. To reduce the reflection of light anti-reflection coating is also applied on top of the *N*-type semiconductor. Normally, many cell are connected in series or series – parallel to get sufficient power and the entire assembly is encapsulate by tempered glass to protect the solar cell from any mechanical shock.

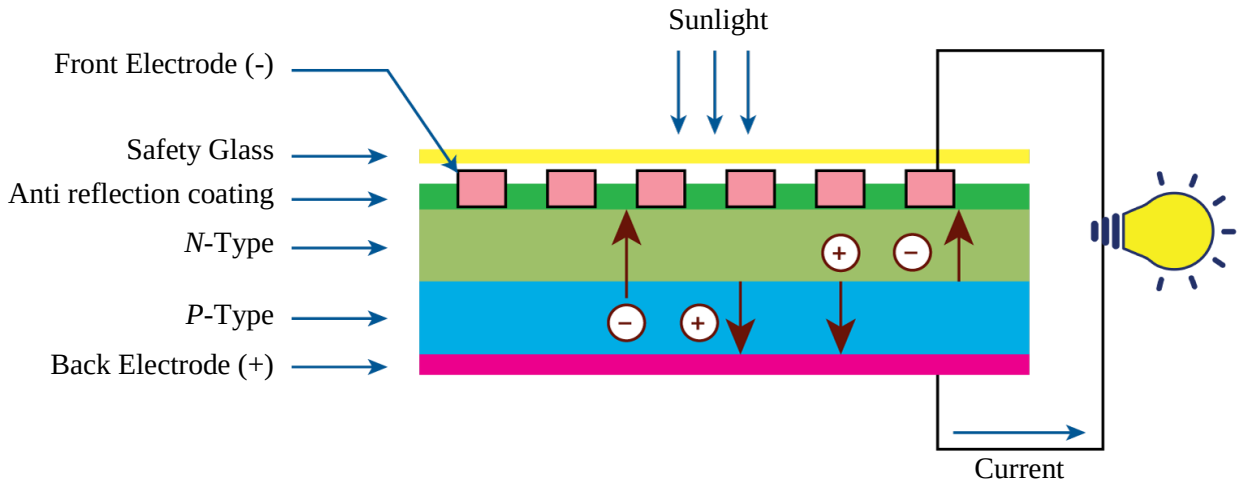


Figure 2.9 Elements of Solar Cell

When light (photons) falls on the cell and reaches the *P-N* junction, it supplies sufficient energy to the junction to create a number of electron-hole (e-h) pairs. This e-h pair creation happens

when light, in the form of photons, impinge the solar cell, photons having sufficient energy (same as band gap of semiconductor) breaks apart electron and raises it to the conduction band leaving behind a hole in the valance band(also known as creation of e-h pair). Each photon with enough energy will normally free exactly one electron, resulting in a free hole as well [10]. Once the e-h pair is created the free electrons in the depletion region are swept away and quickly come to the *N*-type side of the junction due to the electric field in the *P*-*N* junction. Similarly, the holes in the depletion region comes to the *P*-type side of the junction. The electrons in the *N*-type layer is collected by the front electrode and holes in the *P*-type layer is collected by back electrode. Now if there is a connecting path between front and back electrode then current will flow and a closed circuit is formed [11].

2.4 Solar Cell Generations

The evolution of solar cells are categories as solar cell generations and traditionally they are divided into three generations [12]. First generation solar cells are made of silicon wafers. This type of solar cell is the most widely used and manufactured in the world. They also have the highest reported single cell efficiencies. As silicon solar cells are expensive to produce, so researchers are trying to move away from silicon. Second generation solar cells are called thin film solar cells. These solar cells are made of thin film semiconductor materials such as copper indium gallium selenide ($CuIn_xGa_{1-x}Se_2$, CIGS) and cadmium telluride (CdTe). They are lower in cost compared to the silicon cells, but they have environmental issues and the efficiencies are still lower than 1st generation solar cells [13]. Third generation solar cells are much cheaper than all of the other cells, but their efficiencies are much lower than all other cells available. These solar cells are made of materials that do not have a strict *P*-*N* junction like first and second generation cells. Examples of third generation solar cells are dye-sensitized solar cells, perovskite and organic or polymer solar cells. Table 2.1 shows the highest reported efficiencies of each kind of solar cell along with a tandem cell. Tandem cells, also known as multi-junction solar cells, which have more than one *P*-*N* junction and hence more than one cell. They are generally used for space progarms due to their high cost and efficiencies.

TABLE 2.1: Solar Cell Efficiencies [14]

Solar cell	Highest reported efficiency (%)
Silicon (single crystal, single cell)	26.7 ±0.5
CIGS (thin film, single cell)	21.7 ±0.5
CdTe (thin film, single cell)	21.0 ±0.4
Dye-sensitized (single cell)	11.9 ±0.4
Organic polymer (single cell)	11.2 ±0.3
Perovskite (single cell)	20.9±0.7
InGaP/GaAs/InGaAs (tandem cell)	42.3 ±2.5

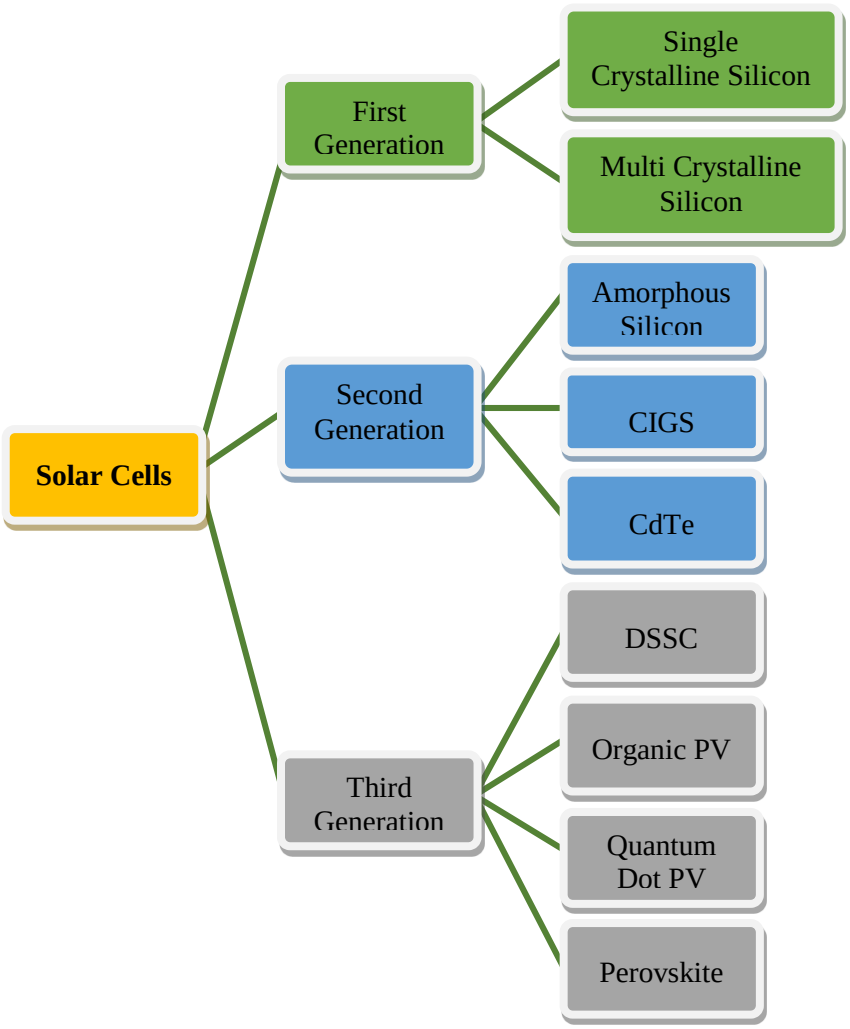


Figure 2.10 Solar Cell Generations

2.4.1 First generation silicon solar cells

Bell Laboratories developed the first silicon solar cell in 1954 with an efficiency of 6%. Since then, research on improving the efficiency and reducing cost of these solar cells has been abundant. Silicon solar cells are the most widely used of all solar cells, and they are also the most efficient in terms of single cell photovoltaic devices. Silicon and it is the most abundant element on earth, only second to oxygen. Silicon has an indirect band gap of 1.12 eV, which allows the material to absorb photons in the visible region of light.

There are two types of silicon used in first generation solar cells. Single crystalline silicon also known as monocrystalline silicon and multicrystalline silicon also known as polycrystalline silicon. As of today single crystalline silicon has the highest efficiency at about 26.7 ± 0.5%, but it is the most expensive. Multicrystalline silicon has a lower efficiency at about 22.3 ± 0.4%, but it is slightly less costly to produce.

2.4.2 Second generation thin film solar cells

Thin film solar cells emerged due to their lower production costs and minimal material consumption, which makes these cells attractive to industry. There are three types of thin film cells. Amorphous silicon, copper indium gallium diselenide ($CuIn_xGa_{1-x}Se_2$, CIGS), and cadmium telluride (CdTe). Amorphous silicon has a much lower efficiency at 10.2 ± 0.3%, but

it is much less expensive to make. Amorphous silicon cells have a couple of disadvantages. One disadvantage is that they do not absorb light as efficiently as other silicon solar cells, and the other is that these cells photodegrade over time. Because of these disadvantages, CIGS and CdTe thin film cells have been developed due to their stability and efficiencies. These cells are also much less expensive to fabricate than amorphous silicon thin film cells.

There are a few fundamental differences between second generation solar cells and first generation solar cells. The most notable difference is the semiconductor material used in the cell has a direct band gap as opposed to the indirect band gap of silicon, but these cells still rely on a *P-N* junction design. Thin film cells have a top layer called the window layer made of a large band gap material that absorbs the higher energy photons and a bottom layer called the absorber layer made of a smaller band gap material that absorbs the lower energy photons, which are not absorbed by the window layer. This design allows for an inherently better efficiency. CIGS cells have the highest efficiencies of thin film cells at 21.7 ± 0.5%; CdTe cells have an efficiency of 21.0 ± 0.4%.

CIGS has a direct band gap which is tunable depending on the ratio of Cu to (In + Ga) and the ratio of In to Ga. $CuInSe_2$ has a band gap of 1.0 eV while $CuGaSe_2$ has a band gap of 1.7 eV. The CIGS layer is the absorber layer of the thin film cell. Cadmium sulfide (CdS), with a larger direct band gap of 2.4 eV, is the window layer of this cell. CdS has been determined as the best window layer material, but ZnS, ZnSe, In_2S_3, ZnO, and MgZnO could also be used as window layer material. The basic structure of a CIGS thin film solar cell is illustrated in Figure 2.11. The glass substrate is typically soda lime glass due to the fact that the sodium diffuses into the CIGS layer and increases conductivity and reduces the formation of lattice defects. Molybdenum (Mo) is used as a back contact for energy flow. The CIGS layer is deposited on the Mo by physical vapor deposition (PVD). A thin CdS layer is then deposited into the CIGS layer by chemical bath deposition (CBD). Both PVD and CBD must be performed at temperatures above 350 °C to ensure crystallinity. A high resistance and low resistance bilayer of ZnO is sputtered onto the cell as transparent conductive oxides. Finally, nickel/aluminum (Ni/Al) contacts are added for energy flow. An anti-reflective coating of MgF_2 is added to maximize the absorption of the photons hitting the cell.

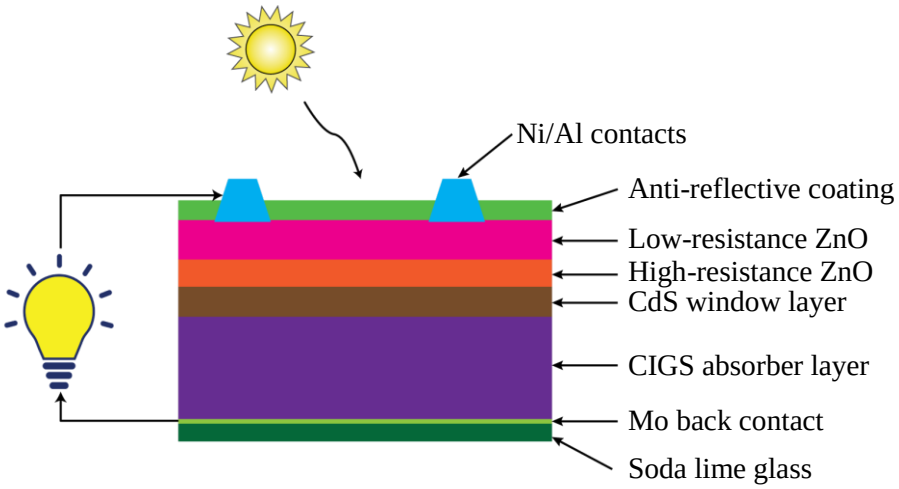


Figure 2.11 CIGS Solar Cell [15]

CdTe thin film cells are very similar to CIGS solar cells. CdTe has a direct band gap of 1.45 eV, and it is used as the absorber layer material. These cells also use CdS as the window layer material. Figure 2.12 illustrates the basic structure of a CdTe solar cell. The glass substrate for this solar cell is typically soda lime glass coated with a thin conductive layer of tin oxide (SnO) or indium tin oxide (ITO). A thin film of CdS is deposited on the glass using the CBD method. The CdTe layer can then be deposited using several different methods. Such as closed-space sublimation (CSS), PVD, electrode position, or spray pyrolysis are all methods of CdTe deposition and all require temperature greater than 400 °C to ensure crystallinity. Finally, a back contact of Mo or W (tungsten) is deposited for conductivity.

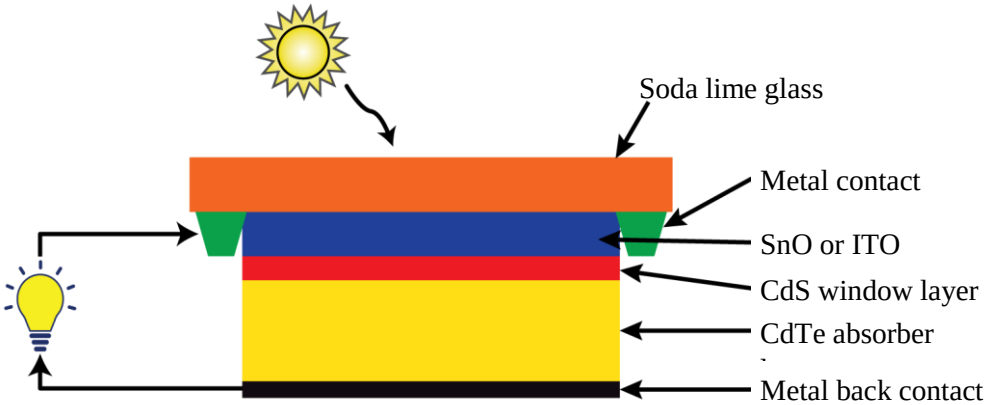


Figure 2.12 CdTe Solar Cell [15]

Although these thin film solar cells have a competitive edge on the first generation solar cells because of lower costs and good efficiencies, they have some drawbacks. Most of the materials used to make these cells are either becoming increasingly rare and more expensive (indium) or are highly toxic (cadmium). For mass production these solar cells would also require new facilities, which would greatly increase the cost of production. Because of these drawbacks the third generation of solar cells have been introduced.

2.4.3 Third generation solar cells

Due to high costs of first generation solar cells and toxicity and limited reserve of materials for second generation solar cells, a new generation of solar cells has emerged. Third generation solar cells are inherently different from the previous two generations because they do not rely on the *P-N* junction design of the others. There are a couple of popular models for third generation cells, which include dye-sensitized solar cells (DSSC) / Grätzel cells, perovskite and organic or polymer solar cells.

2.4.4 Multi-junction or tandem cells

A tandem cell, by definition, consists of at least two *P-N* junctions with cells composed of materials that absorb different photon energies. The top cell would absorb the higher energies while the bottom cell would absorb the lower energies that are not absorbed by the top cell, similar to the principle behind thin film cells. The tandem cell would, then have a higher efficiency as it could absorb more photons of the solar spectrum for energy conversion. This technology is already being put to use in solar cells in space. Tandem solar cells are typically

made of compounds of elements in the III and V groups of the periodic tables. Examples of these compounds are gallium arsenide (GaAs), indium phosphide (InP), gallium antimonide (GaSb), gallium indium phosphide (GaInP), and gallium indium arsenide (GaInAs). These solar cells have the highest reported efficiency at 43% when using a three junctions solar cell, but they use rare metals and are extremely expensive to fabricate, so they are used for terrestrial purpose in large scale.

2.5 Equivalent Circuit of a Solar Cell

To understand the electronic behavior of a solar cell, it is useful to create a model which is electrically equivalent, and is based on discrete electrical components whose behavior is well known. An ideal solar cell may be modelled by a current source in parallel with a diode; in practice no solar cell is ideal, so a shunt resistance and a series resistance component are added to the model [16]. The resulting equivalent circuit of a solar cell is shown on the Figure 2.13.

From the equivalent circuit, it is evident that the current produced by the solar cell is equal to that produced by the current source, minus that which flows through the diode, minus that which flows through the shunt resistor. That is

$I = I_P - I_D - I_{SH}$ ……(1)

Where,

I = output current (amperes)

I_P = photogenerated current (amperes)

I_D = diode current (amperes)

I_{SH} = shunt current (amperes).

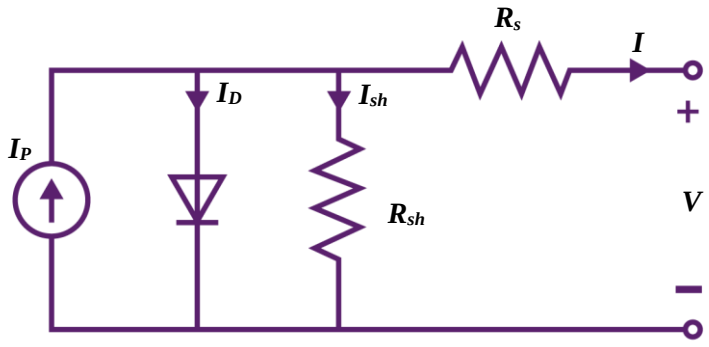


Figure 2.13 The Equivalent Circuit of a Solar Cell [17]

The current through these elements is governed by the voltage across them:

$V_j = V + IR_S$ ……(2)

Where,

V_j = voltage across both diode and resistor R_{SH} (volts)

V = voltage across the output terminals (volts)

I = output current (amperes)

R_S = series resistance (Ω).

By the Shockley diode equation, the current diverted through the diode is:

$$I_D = I_0 \{ exp [\frac{qVj}{nkT}] - 1 \} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Where,

- I_0 = reverse saturation current (amperes)
- n = diode ideality factor (1 for an ideal diode)
- q = elementary charge
- k = Boltzmann's constant
- T = absolute temperature
- At 25°C, $\frac{kT}{q} \approx$ 0.0259 volts.

By Ohm's law, the current diverted through the shunt resistor is:

$$I_{SH} = \frac{V_j}{R_{SH}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Where,

- R_{SH} = shunt resistance (Ω).

Substituting these into the first equation produces the characteristic equation of a solar cell, which relates solar cell parameters to the output current and voltage:

$$I = I_L - I_0 \{ exp [\frac{q(V+IR_S)}{nkT}] - 1 \} - \frac{V+IR_S}{R_{SH}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (5) [18]$$

2.5.1 Open-circuit voltage and short-circuit current

When the cell is operated at open circuit, I = 0 and the voltage across the output terminals is defined as the open-circuit voltage. Assuming the shunt resistance is high enough to neglect the final term of the characteristic equation and n = 1, the open-circuit voltage V_{oc} is:

$$V_{oc} \approx \frac{kT}{q} ln (\frac{I_l}{I_0} + 1) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

Similarly, when the cell is operated at short circuit, $V = 0$ and the current I through the terminals is defined as the short-circuit current. It can be shown that for a high-quality solar cell (low R_S and I_0, and high R_{SH}) the short circuit current I_{sc} is:

$$I_{sc} \approx I_P \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$$

The values of I_0, R_S, and R_{SH} are dependent on the physical size of the solar cell. In comparing otherwise identical cells, a cell with twice the surface area of another will, in principle, have double the I_0 because it has twice the junction area across which current can leak. It will also have half the R_S and R_{SH} because it has twice the cross-sectional area through which current can flow. For this reason, the characteristic equation is frequently written in terms of current density, or current produced per unit cell area:

$$J = J_L - J_0 \{ exp [\frac{q(V+Jr_s)}{nkT}] - 1 \} - \frac{V+Jr_S}{r_{SH}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

Where,

J = current density (amperes/cm^2)

J_L = photogenerated current density (amperes/cm^2)

J_0 = reverse saturation current density (amperes/cm^2)

r_S = specific series resistance (Ω-cm^2)

r_{SH} = specific shunt resistance (Ω-cm^2).

This formulation has several advantages. One is that since cell characteristics are referenced to a common cross-sectional area they may be compared for cells of different physical dimensions. While this is of limited benefit in a manufacturing setting, where all cells tend to be the same size, it is useful in research and in comparing cells between manufacturers. Another advantage is that the density equation naturally scales the parameter values to similar orders of magnitude, which can make numerical extraction of them simpler and more accurate even with naive solution methods.

There are practical limitations of this formulation. For instance, certain parasitic effects grow in importance as cell sizes shrink and can affect the extracted parameter values. Recombination and contamination of the junction tend to be greatest at the perimeter of the cell, so very small cells may exhibit higher values of J_0 or lower values of r_{SH} than larger cells that are otherwise identical. This approach should only be used for comparing solar cells with comparable layout. For instance, a comparison between primarily quadratical solar cells like typical crystalline silicon solar cells and narrow but long solar cells like typical thin film solar cells can lead to wrong assumptions caused by the different kinds of current paths and therefore the influence of for instance a distributed series resistance r_S.

2.6 Solar Cell *I-V* Characteristic Curves

Solar Cell *I-V* characteristic curve shows the current and voltage (*I-V*) characteristics of a particular solar cell and gives a detailed description of its solar energy conversion ability and efficiency [19]. Knowing the electrical *I-V* characteristics (more importantly P_{max}) of a solar cell is critical in determining the device's output performance and conversion efficiency.

Solar Cell *I-V* characteristic curves are basically a graphical representation of the operation of a solar cell summarizing the relationship between the current and voltage at the existing conditions of irradiance and temperature. *I-V* curves provide the information required to configure a solar system so that it can operate as close to its optimal peak power point (MPP) as possible.

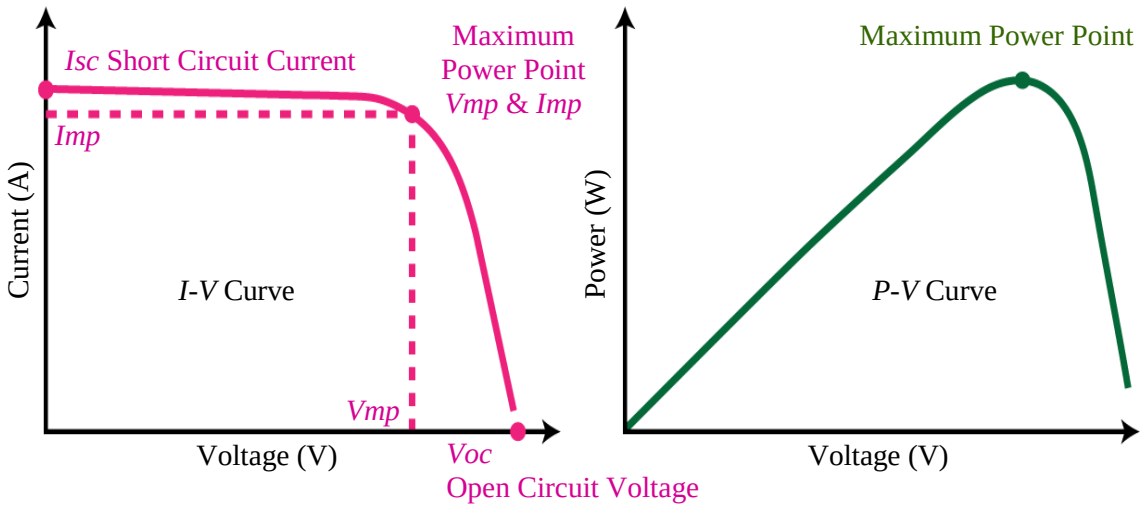


Figure 2.14 *I-V* and *P-V* Curves of Solar Cell

The above graph (Figure 2.14) shows the current-voltage (*I-V*) characteristics of a typical silicon PV cell operating under normal irradiance conditions. The power delivered by a solar cell is the product of current and voltage (I × V). If the multiplication is done, point by point, for all voltages from short-circuit to open-circuit conditions, the power curve of Figure 2.14 is obtained for a given radiation level.

In open – circuit condition that is, when the cell is not connected to any load, the current will be at its minimum (zero) value and the voltage across the cell is at its maximum value, known as the solar cells open circuit voltage, or V_{oc}. At the other extreme, when the solar cell is short circuited, that is the positive and negative leads are connected together, the voltage across the cell is at its minimum (zero) value but the current flowing out of the cell reaches its maximum value, known as the solar cell short circuit current, or I_{sc}.

Then the span of the solar cell *I-V* characteristics curve ranges from the short circuit current (I_{sc}) at zero output volts, to zero current at the full open circuit voltage (V_{oc}). In other words, the maximum voltage available from a cell is at open circuit, and the maximum current at closed circuit. Of course, neither of these two conditions generates any electrical power, but there must be a point somewhere in between where the solar cell generates maximum power.

However, there is one particular combination of current and voltage for which the power reaches its maximum value, at I_{mp} and V_{mp}. The maximum value, at I_{mp} and V_{mp} is known as maximum power point as shown in Figure 2.14. The "maximum power point" or MPP is the ideal operation of a photovoltaic cell (or panel). It is to be mentioned that since solar cell output voltage and current both depend on temperature, the actual output power will vary with changes in ambient temperature.

2.6.1 Fill Factor and Efficiency of Solar Cell

The short-circuit current (I_{sc}) and the open-circuit voltage (V_{oc}) are the maximum current and voltage respectively from a solar cell. However, at both of these operating points, the power from the solar cell is zero. The "*fill factor*", more commonly known by its abbreviation "*FF*", is a parameter which, in conjunction with V_{oc} and I_{sc}, determines the maximum power from a solar cell. The *FF* is defined as the ratio of the maximum power from the solar cell to the product of V_{oc} and I_{sc}. Graphically, the *FF* is a measure of the squareness of the solar cell and

is also the area of the largest rectangle which will fit in the IV curve. The FF is illustrated in Figure 2.15.

Graph of cell output current (red line) and power (blue line) as function of voltage is shown in Figure 2.15. Also shown are the cell short-circuit current (I_{sc}) and open-circuit voltage (V_{oc}) points, as well as the maximum power point (V_{mp}, I_{mp}).

As *FF* is a measure of the squareness of the IV curve, a solar cell with a higher voltage has a larger possible *FF* since the rounded portion of the IV curve takes up less area. The equation for Fill Factor is given below:

$$FF = \frac{V_{max} I_{max}}{V_{OC} I_{SC}} \ldots\ldots\ldots\ldots (9)$$

Where *FF* is the fill factor, V_{oc} is the open circuit voltage, I_{sc} is the short circuit current, V_{max} is the voltage at maximum output, I_{max} is the amperage at maximum output.

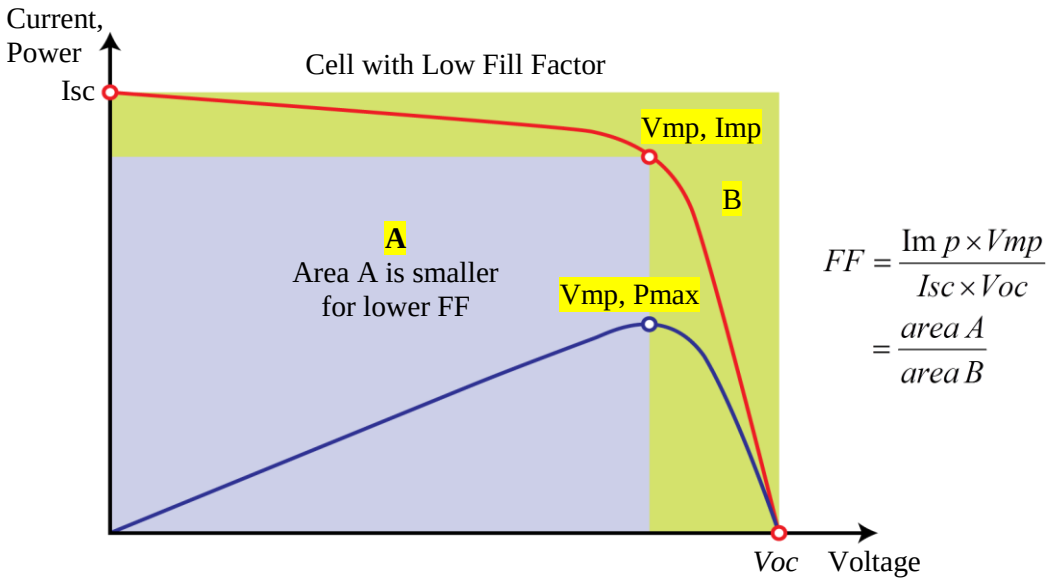


Figure 2.15 Fill Factor [20]

The efficiency is the most commonly used parameter to compare the performance of one solar cell to another. Efficiency is defined as the ratio of power output from the solar cell to input power from the sun. The equation for efficiency is given below:

$$\eta = \frac{V_{max} I_{max}}{P_{in}} \ldots\ldots\ldots\ldots (10)\ [21]$$

$$\eta = \frac{V_{OC} I_{SC} FF}{P_{in}} \ldots\ldots\ldots\ldots (11)$$

Where, P_{in} is the input power (solar irradiation) and η is the efficiency of solar cell. Normally the input power for efficiency calculations is considered to be 1 kW/m^2 or 100 mW/cm^2. Thus the input power for a 100 × 100 mm^2 cell is 10 W and for a 156 × 156 mm^2 cell is 24.3 W.

2.7 Materials for Solar Cell Fabrication

There are three types of technologies available on the market today. Which are monocrystalline/single crystal cells, polycrystalline/multicrystalline, and thin film [22]. As

the names suggest both the monocrystalline and polycrystalline types of solar cells are made from crystalline silicon. Details about all these materials used in the solar cell fabrication are given below.

2.7.1 Monocrystalline

2.7.1.1 Overview

This is the oldest and most developed of the three technologies. Monocrystalline panels as the name suggests are created from a single continuous crystal structure [23]. Single-crystalline wafers typically have better material parameters but are more expensive. Crystalline silicon has an ordered crystal structure, with each atom ideally lying in a pre-determined position. Crystalline silicon exhibits predictable and uniform behaviour but as it needs careful and slow manufacturing processes, it is also the most expensive type of silicon.

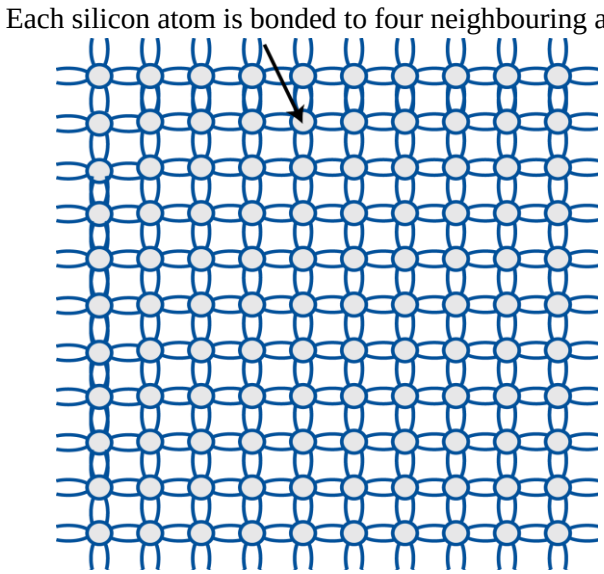


Figure 2.16 Regular Arrangement of Silicon Atoms in Single-Crystalline Silicon

Figure 2.16 shows the regular arrangement of silicon atoms in a single-crystalline silicon, that produces a well-defined band structure. Each silicon atom has four electrons in the outer most shell and forms four co-valent bond with four neighbouring atoms.

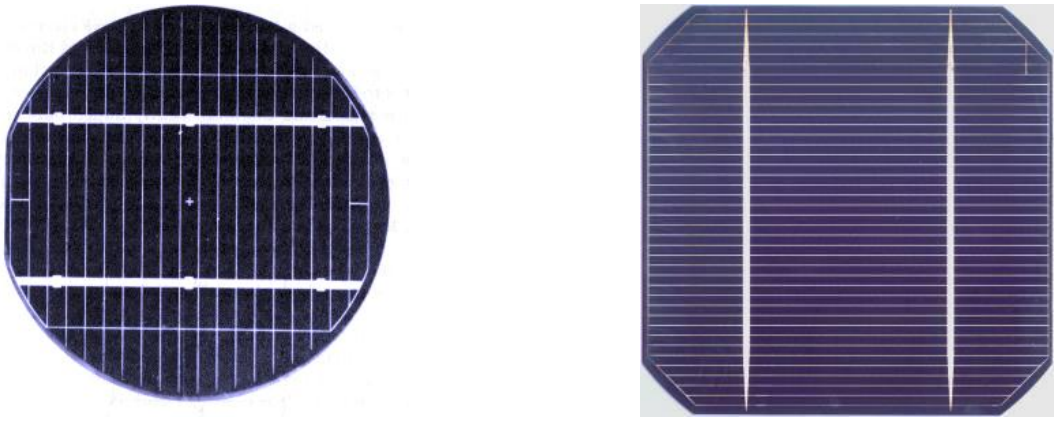
2.7.1.2 Construction

Single-crystalline silicon are made through the Czochralski method where a silicon crystal seed is placed in a vat of molten silicon. The seed is then slowly rotated and drawn up with the molten silicon forming a solid crystal structure around the seed known as an ingot. The ingot of solid crystal silicon that is formed is then finely sliced and is known as a silicon wafer. This wafer used to make solar cell.

The Czochralski process results in large cylindrical ingots producing circular or semi-square/pseudo square solar cells (as shown in Figure 2.17). The semi-square cell started out circular but has the edges cut off that is four sides are cut out of the ingots to make silicon wafers. For this reason a significant amount of the original silicon ends up as waste. Pseudo square solar cells can be packed more efficiently than circular solar cells into a module.

2.7.1.3 Orientation

In single crystalline silicon material the crystal orientation is defined by Miller indices. A particular crystal plane is noted using parenthesis such as (100). Silicon has a cubic symmetrical cubic structure and so (100), (010) etc are equivalent planes and collectively referred to using braces {100}. Similarly, the crystal directions are defined using square brackets, e.g. [100] and referred collectively using triangular brackets, <100>.



(a) (b)

Figure 2.17 (a) Circular Monocrystalline Solar Cell (b) Pseudosquare Monocrystalline Solar Cell

In solar cell fabrication the preferred orientation is <100> as this can be easily textured to produce pyramids that reduce the surface reflectivity. Texturing causes (111) plane to from on the surface (100) plane. To denote the crystal directions, single crystal wafers often have flats to denote the orientation and doping type of the wafer. Flats are of two types and they are primary (major) flat and secondary (minor) flat. Primary flat is defined as the flat of longest length located in the circumference of the wafer. With the help of secondary flat the crystal orientation and doping of the wafer can be identified.

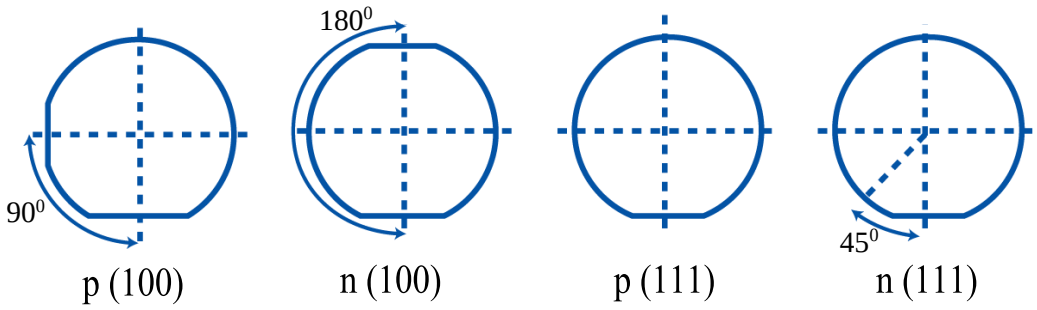


Figure 2.18 Orientation and Doping Type Determination Using Major and Minor Flats

Normally to identify orientation and doping type the Semiconductor Equipment and Materials International (SEMI) standard is used (Figure 2.18). The standard is given below:

- If the minor flat is 180° from the major flat the wafer is *N*-type <100>
- If the minor flat is 90° to the left or right the wafer is *P*-type <100>.
- If the minor flat is 45° up on the left or right the wafer is *N*-type <111>
- If there are no minor flats the wafer is *P*-type <111>

2.7.2 Polycrystalline or Multicrystalline

2.7.2.1 Overview

Polycrystalline solar cells are made from polycrystalline silicon wafers. A polycrystaline material, as the name suggests, is composed of many crystals joined together. Polycrystalline materials are solids that are composed of many crystallites of varying size and orientation. The orientation of the crystals (also referred to as grains) are different from each other. For example a Silicon wafer of (100) orientation would be obtained from a single crystal which has a large single grain of (100) orientation. On the other hand, a crystalline material consisting of many grains of different orientation is called polycrystalline. The grains are small or even microscopic crystals and are formed during the cooling of many materials. The grain boundary of polycrystalline material are shown in Figure 2.19.

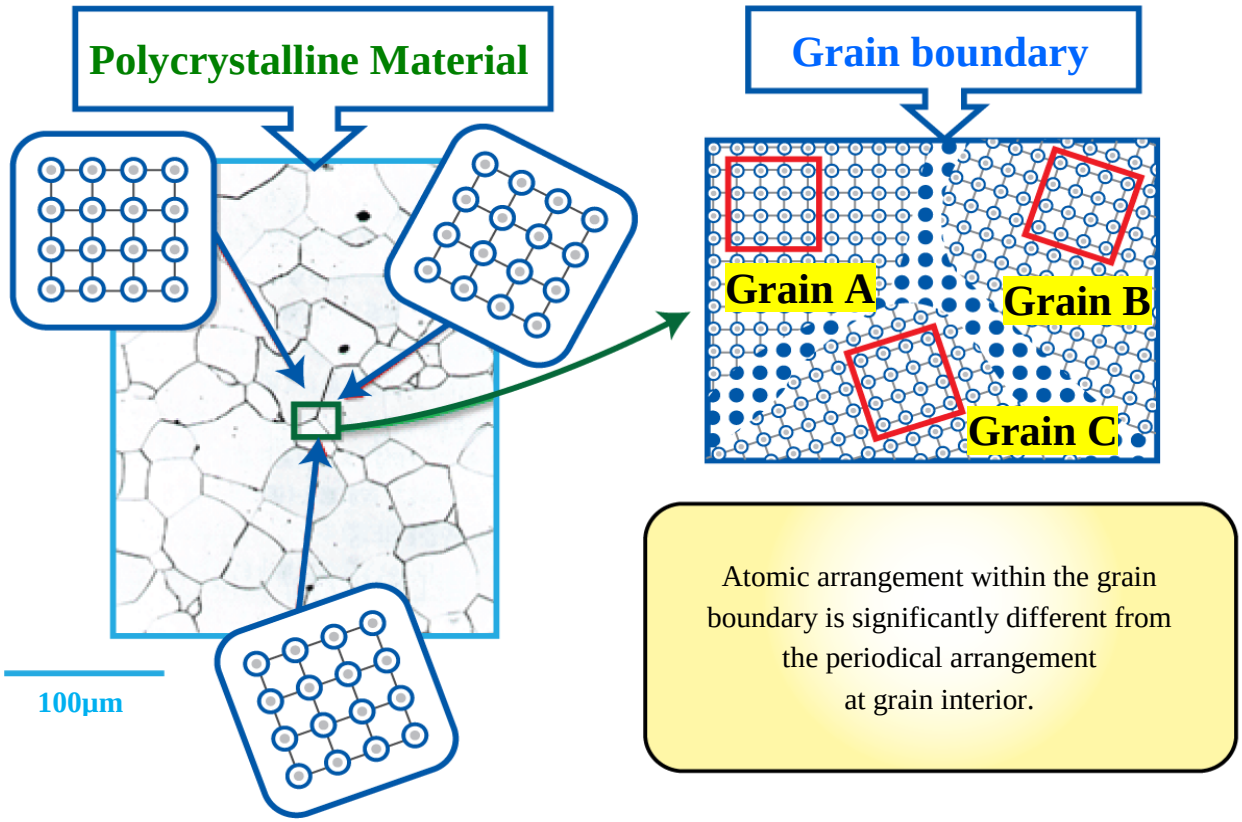


Figure 2.19 The Grain Boundary of Polycrystalline Material [24]

2.7.2.2 Construction

Polycrystalline also starts as a silicon crystal seed placed in a vat of molten silicon. However, rather than drawing the seed up as with Monocrystalline, the vat of silicon is simply allowed to cool. This is what forms the distinctive edges and grains in the solar cell.

2.7.3 Thin Film

The technology of thin film panel is a totally different technology to Mono and Polycrystalline panels. This is a new technology compared to Mono and Polycrystalline cells and would not

be considered a mature technology as vast improvements in this technology are expected in the next 10 years.

2.7.3.1 Construction

Thin film panels are made by depositing a photovoltaic substance onto a solid surface like glass. The photovoltaic substance that is used varies and multiple combinations of substances have successfully and commercially been used. Examples of the most common photovoltaic substances used are:

- Amorphous Silicon
- Cadmium Telluride (CdTe)
- Copper indium gallium selenide (CIGS)

Each of the above are known as different panel types but all fall under the umbrella of Thin Film panel.

2.7.4 Identification of Monocrystalline, Polycrystalline & Thin Film by Visualization

Identifying of monocrystalline, polycrystalline and thin film solar panels by visualization is difficult. However sometimes it can be done so. Normally a monocrystalline solar panel can be identified from the solar cells which all appear as a single flat color [25]. A thin film panel can be identified as having a solid black appearance. They may or may not have a frame, if the panel has no frame it is a thin film panel. The internal crystal (grain) boundaries is some time visible in polycrystalline solar cells (Figure 2.20).

Another way is to look at the shape of the cell. Usually monocrystalline cells have rounded shape corners (pseudo Square or circular, Figure 2.17) whereas the polycrystalline cells are square. This is due to the fabrication process. Sometimes solar panels are black in color. This blackness is due to Broad Band Anti-Reflective (BBAR) coatings. The black solar panels maybe identified via shape of the cell as stated earlier.

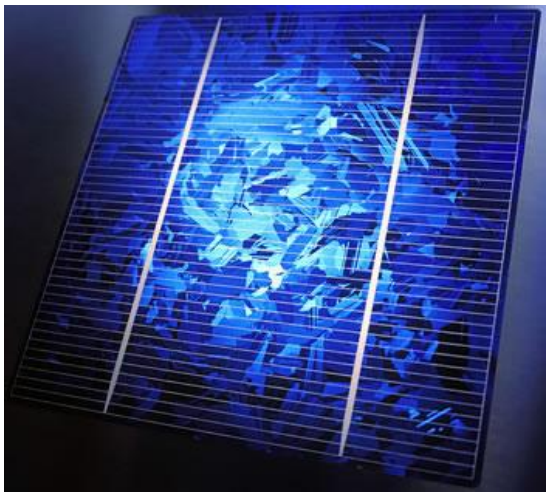


Figure 2.20 Polycrystalline Solar Cell

2.8 Criterion Parameters of Solar Cell

To determine the performance of a solar cell, it is very crucial to know about the parameters of a solar cell. The parameters of solar cell not only evaluates the performance but also very much

required for design and fabrication of solar cell. Especially, in case of solar cell simulation without proper knowledge of the parameters accurate solar cell modelling is difficult. Thus some of the important solar cell parameters required for evaluating performance, designing solar cell in simulation and practical purpose are described in the following section.

2.8.1 Emitter and Base

The substrate material used in the solar cell fabrication is called the base. Normally the base is a *P*-type material. Upon the base *N*-type material is grown and the *N*-type material is called the emitter. An absorber material (base) is typically a moderately doped *P*-type square wafer having thickness around 300 μm and an area of 10×10 cm^2 or 12.5×12.5 cm^2. The base thickness varies form 100 μm to 500 μm. Whereas the thickness of emitter is ≤ 3 μm, normally it is 2 or 1 μm. A large fraction of light is absorbed close to the front surface. By making the emitter very thin, a large fraction of the carriers generated by the incoming light are created within a diffusion length of the *P*-*N* junction.

2.8.2 Grid Pattern

In addition to semiconductor layers, solar cells consist of a top and bottom metallic grid that collects the electric current. The wide vertical strips of the grid pattern is known as busbars and the horizontal thin strips are called grid-fingers. The resistivity of silicon is too low to conduct away all the current generated, so a lower resistivity metal grid is placed on the surface to conduct away the current. The metal grid shades the cell from the incoming light so there is a compromise between light collection and resistance of the metal grid. Generally the grid-fingers are of 20 to 200 μm width, and placed 1 - 5 mm apart.

2.8.3 Doping

The concentrations of electrons and holes in crystalline silicon (c-Si) can be manipulated by doping. By doping c-Si it is meant that atoms of appropriate elements substitute Si atoms in the crystal lattice. The substitution has to be carried out by atoms with three or five valence electrons, such as boron or phosphorous, respectively. The doping action can best be understood with the aid of the bonding model and is demonstrated in Figure 2.21. When introducing phosphorous atom into the c-Si lattice, its four of the five valence electrons will readily form bonds with the four neighbouring Si atoms. The fifth valence electron cannot take part in forming a bond and becomes rather weakly bound to the phosphorous atom. It is easily liberated from the phosphorous atom by absorbing the thermal energy, which is available in the c-Si lattice at room temperature. Once free, the electron can move throughout the lattice. In this way, the phosphorous atom that substitutes a Si atom in the lattice donates a free (mobile) electron into the c-Si lattice. The impurity atoms that enhance the concentration of electrons are called donors. The concentration of donors is denoted by N_D. An atom with three valence electrons, such as boron, cannot form all bonds with four neighbouring Si atoms when it substitutes a Si atom in the lattice. Thus it can readily accept an electron from a nearby Si-Si bond. A thermal energy that the c-Si lattice contains at room temperature is sufficient to enable an electron from a nearby Si-Si bond to attach itself to the boron atom and complete the bonding to the four Si neighbours.

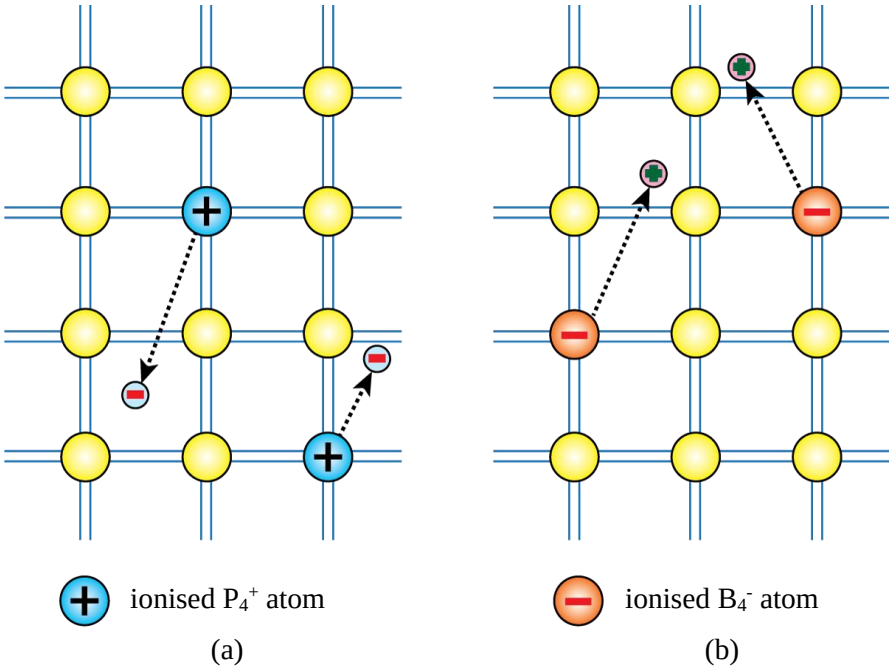


Figure 2.21 Doping Process Illustration Using the Bonding Model. (a) A Phosphorus Atom Substitutes a Si Atom in the Lattice Resulting in the Positively-Ionised Phosphorus Atom and a Free Electron, (b) A Boron Atom Substitutes a Si Atom Resulting in the Negatively Ionised Boron Atom and a Hole [26]

In this way, a hole is created that can move around the lattice. The impurity atoms that enhance the concentration of holes are called acceptors. The concentration of donors is denoted by N_A. By substituting Si atoms with only one type of impurity atoms, the concentration of only one type of mobile charge carriers is increased. Charge neutrality of the material is nevertheless maintained because the sites of the bonded and thus fixed impurity atoms become charged. The donor atoms become positively ionised and the acceptor atoms become negatively ionised.

A possibility to control the electrical conductivity of a semiconductor by doping is one of most important semiconductor features. The electrical conductivity in semiconductors depends on the concentration of electrons and holes and their mobility. The concentration of electrons and holes is influenced by the amount of the impurity atoms that are introduced into the atomic structure of semiconductor. A moderately-doped *P*-type c-Si has an acceptor concentration of 10^{16} cm^{-3}.

2.8.3.1 Doping of base

A higher base doping leads to a higher V_{oc} and lower resistance, but higher levels of doping result in damage to the crystal. The doping of base is such that it has resistivity around 1 Ω·cm.

2.8.3.2 Doping of emitter

The front junction is doped to a level sufficient to conduct away the generated electricity without resistive loses. However, excessive levels of doping reduces the quality of material to the extent that carriers recombine before reaching the junction. The doping of emitter is around 100 Ω/□ (Ohm/square).

2.8.4 Carrier Concentration

At 300°K there are approximately 1.5×10^{10} broken bonds per cm^3 in the intrinsic crystalline silicon (c-Si). This number then gives also the concentration of holes, *p*, and electrons, *n*, in the intrinsic c-Si. It means, that at 300°K $n = p = 1.5 \times 10^{10}$ cm^{-3}. This concentration is called the intrinsic carrier concentration and is denoted by n_i. The total concentration of electrons in the conduction band and the total concentration of holes in the valence band is obtained by

$$n = N_C \exp\left[\frac{E_F - E_C}{KT}\right] \text{ for } E_c - E_F \geq 3kT \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (12)$$

$$p = N_v \exp\left[\frac{E_v - E_C}{KT}\right] \text{ for } E_F - E_v \geq 3kT \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (13)$$

Where, N_C and N_V are the effective density of conduction band states and the effective density of valence band states, respectively. In c-Si, $N_C = 3.22 \times 10^{19}$ cm^{-3} and $N_V = 1.83 \times 10^{19}$ cm^{-3} at 300°K. When that the Fermi Level lies in the band gap more than 3*kT* from either band edge the semiconductor is referred to as non-degenerate. In an intrinsic semiconductor in the equilibrium $n = p = n_i$ ……. (14)

Where *k* is Boltzmann constant ($k = 1.38 \times 10^{-23}$ JK^{-1}) and F_E is the so-called Fermi energy. *kT* is expressed in *eV* and equals to 0.0258 eV at 300° K. The Fermi energy is the electrochemical potential of the electrons in a material and in this way it represents the average energy of electrons in the material.

The concentrations of electrons and holes in c-Si can be manipulated by doping. The concentration of electrons and holes is influenced by the amount of the impurity atoms that substitute silicon atoms in the lattice. Under the assumption that the semiconductor is uniformly doped, in equilibrium, a simple relationship between the carrier and dopant concentrations can be established. Assuming that at room temperature the dopant atoms are ionized, inside a semiconductor the local charge density is given by:

$$\rho = q\,(p + N^+_D - n - N^-_A) \quad \ldots\ldots\ldots\ldots\ldots\ldots (15)$$

Where *q* is the elementary charge ($q = 1.602 \times 10^{-19}$ C). Under equilibrium conditions, in the uniformly doped semiconductor the local charge is zero, which means that the semiconductor is everywhere charge-neutral. It can be written as

$$p + N^+_D - n - N^-_A = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (16)$$

As previously discussed, the thermal energy available at room temperature is sufficient to ionise almost all the dopant atoms. Under this assumption, $N^+_D \approx N_D$ and $N^-_A \approx N_A$, one obtains

$$p + N_D - n - N_A = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (17)$$

Which is the common form of the charge neutrality equation.

2.8.5 Diffusion Coefficients

The constants of proportionality, D_N and D_P, are referred to as electron and hole diffusion coefficients, respectively. The diffusion coefficients of electrons and holes are linked with the mobilities of the corresponding charge carriers by the Einstein relationship, which is expressed as

$\frac{D_N}{\mu_n} = \frac{KT}{q}$ …… (18)

$\frac{D_P}{\mu_p} = \frac{KT}{q}$ …… (19)

2.8.6 Diffusion Length

When light falls upon the solar cell it is simple enough to think that *e-h* pair is generated in the *P-N* junction and due to the electric field in the *P-N* junction the *e-h* pair are forced out from the PN junction and the e-h pair are collected from the output terminal to get current. However, light does not only falls one *P-N* junction then fall in *P*-type and *N*-type region also. So in those region *e-h* pair are also generated also. However, the *e-h* pair generated in *P*-type and *N*-type region first tries to go to the *P-N* junction then if they reach it due to the electric field they come out from the terminal and current is obtained. But not all the *e-h* pair generated in *P*-type and *N*-type region can reach the *P-N* junction. Some of the *e-h* pair generated in *P*-type and *N*-type region recombines and generate heat before reaching the *P-N* junction. So if light falls on *P*-type and *N*-type region of solar cell then the length up to which the *e-h* pair can go to the *P-N* junction is called diffusion length. Now if the diffusion length is high then more *e-h* pair will go to the *P-N* junction thus come out of the terminal and increase the efficiency of solar cell. If diffusion length is low then recombination will happen more before *e-h* pair will go to the *P-N* junction thus reducing the efficiency of solar cell. The minority-carrier-diffusion lengths are defined as:

$L_N = \sqrt{D_n \tau_n}$ …… (20) for electrons in a *P*-type material

$L_p = \sqrt{D_p \tau_p}$ …… (21) for holes in an *N*-type material

2.8.7 Air Mass 1.5 G

AM (Air Mass) 1.5 G condition is defined as equal to 100 mW/cm^2 or 1000 W/m^2 of irradiance. AM 1.5 standard spectra are defined by the American Society for Testing and Materials

2.9 Shockley–Queisser Limit

In physics, the Shockley–Queisser limit, also known as the detailed balance limit, Shockley Queisser Efficiency Limit or SQ Limit, refers to the maximum theoretical efficiency of a solar cell using a single *P-N* junction to collect power from the cell. It has been first calculated by William Shockley and Hans-Joachim Queisser at Shockley Semiconductor in 1961 [27]. The limit is one of the most fundamental to solar energy production with photovoltaic cells, and is considered to be one of the most important contributions in the field.

The limit is that the maximum solar conversion efficiency is around 33.7% for a single *P-N* junction photovoltaic cell, assuming typical sunlight conditions (unconcentrated, AM 1.5 solar spectrum), and subject to other caveats and assumptions discussed below. This maximum occurs at a band gap of 1.34 eV (Figure 2.22) [28]. That is, of all the power contained in sunlight (about 1000 W/m²) falling on an ideal solar cell, only 33.7% of that could ever be turned into electricity (337 W/m²). The most popular solar cell material, silicon, has a less favorable band gap of 1.1 eV, resulting in a maximum efficiency of about 32%. Modern commercial mono-crystalline solar cells produce about 24% conversion efficiency, the losses due largely to

practical concerns like reflection off the front of the cell and light blockage from the thin wires on the cell surface.

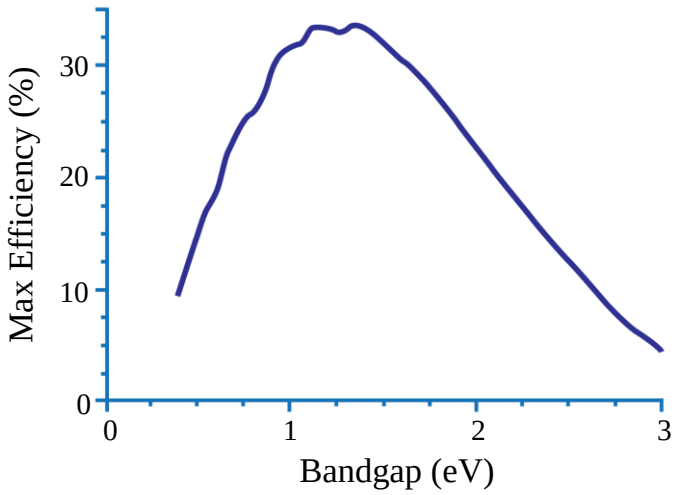


Figure 2.22 Solar Cell Conversion Efficiency

The Shockley–Queisser limit only applies to conventional solar cells with a single *P-N* junction. Tandem solar cells with multiple layers can (and do) outperform this limit, and so can solar thermal and certain other solar energy systems. In the extreme limit, for a tandem solar cell with an infinite number of layers, the corresponding limit is 86.8% using concentrated sunlight [29].

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Chapter 3

CHARACTERIZATION AND FABRICATION EQUIPMENT

3.1 Introduction

Knowledge about characterization and fabrication equipment is very much required for solar cell fabrication and for solar cell performance analysis process. Thus in this chapter the equipment that are used for characterization and fabrication of solar cell in Bangladesh are briefly discussed.

3.2 Lux Meter

A lux meter is an equipment that measures brightness of falling light on an object at a particular area [1]. In other words, it properly measuress the intensity at which brightness the object appears to the human eye. Lux can be simply defined as a unit of measurement of illuminance or more accurately, brightness. It derives its name from the candela, which is the standard unit of measurement for the power of light.

Figure 3.1 CEM DT-8809A Lux Meter

Generally in the solar panel testing laboratory the input power (P_{in}) is created artificially and considered Air-mass 1.5 G condition. That is 1000 Watt/m^2 [2]. However, in case of measurement under the real sun, 1000 Watt/m^2 cannot be always considered as the intensity of the sun varies. However, it is possible to calculate the solar cell input power (P_{in}) using lux meter under direct sun condition. The lux meter measures luminous flux per unit area. So this

illuminance in lux (lx) needs to be converted in watts (W). The lux to watt (W) conversion is done using the following equation:

$$P_{in}\ (W) = \frac{E_V(lx) \times A_{m^2}}{\eta_{(\frac{lm}{w})}} \quad \ldots\ldots\ldots (1)\ [3]$$

Where $E_V(lx)$ is illuminance (E_V) in lux (lx), A is the surface area of solar panel in square meter (m^2) and η is the luminous efficacy in lumens per watt ($\frac{lm}{w}$). The input power is always measured in sunny condition. Here, the luminous efficacy of day light is considered 105 ($\frac{lm}{w}$) [4-6].

3.3 Particle Counter

A particle counter is an instrument that detects and counts physical particles. Particle counters for air and gas are crucial for the cleanroom industry [7]. That is a particle counter measures the cleanliness level of cleanroom and controlled environments for sensitivity and contamination analysis. Here, in this research a Met One A2400 LASER particle counter [8] (as shown in Figure 3.2) has been used to measure the cleanliness level of the solar cell fabrication laboratory at Bangladesh Atomic Energy Commission, Savar, Bangladesh.

Figure 3.2 Met One A2400 LASER Particle Counter

3.4 Dial Indicator

Dial indicator is a device to measure the thickness of thin samples, especially textured and raw wafer. A Mitutoyo dial indicator [9], model no- 2110S-10, Japan (Figure 3.3) has been used for measuring the thickness of the samples. This dial indicator can measure the thickness in the micron range.

Figure 3.3 Dial Indicator

To measure thickness the dial indicator must be placed in a flat surface. Then the outer dial face must be rotated so that the hand hovers over zero. Then the sample is placed under the contact point and the outer (larger) gauge hand is rotated clockwise. Here, the larger gauge represents a smaller measurement. The outer gauge face has 100 notches. For every 100 rotation in the outer gauge, the inner gauge indicator rotates 1 step counter clockwise. After adding both the small gauge and large gauge measurements, the thickness of the sample can be obtained.

3.5 Weighing Scales

Weighing scales are devices to measure weight. Here two types of weight scales have been used.

(a) (b)

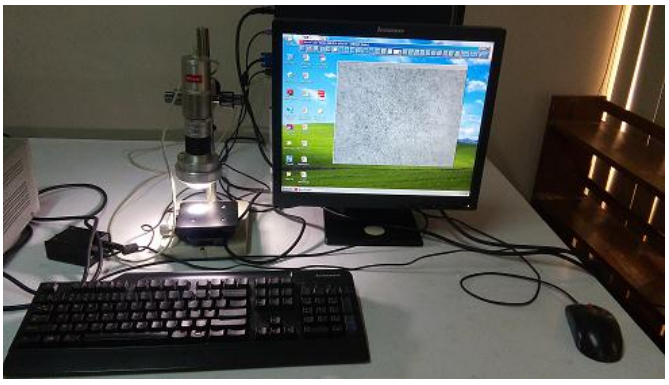
Figure 3.4 (a) A&D HL-100 Precision Balance (b) A&D GR-200 Analytical Balance

For texturization process, different chemicals have been used and the chemical pallets weight has been measured using A&D HL-100 Precision Balance system (as shown in Figure 3.4 (a)). This system can measure weight up to two decimal point [10]. This is a very good instrument for measuring chemical pallets. However this device cannot be used to measure the weight of small textured samples. Thus, to measure the weight of raw (*P*-type monocrystalline substrate) and textured wafer samples A&D GR-200 Analytical Balance has been used (as shown in Figure 3.4 (b)). The analytical balance can measure weight up to four decimal point [11]. Also it is a closed system, that is, to protect the samples form dust (the dust increases the weight) the samples are kept in a closed environment. Both devices are operated by electricity.

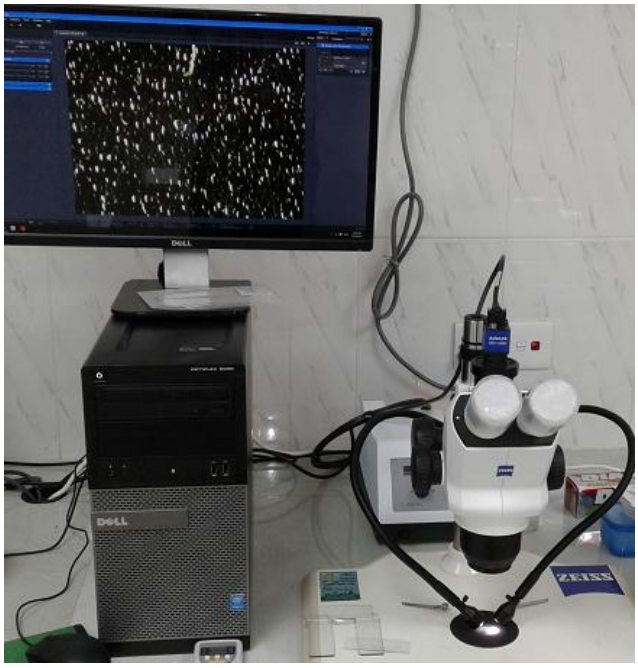
3.6 Optical Microscope

The optical microscope, often referred to as the light microscope, is a type of microscope that uses visible light and a system of lenses to magnify images of small subjects. Here, total four types of optical microscopes have been used to inspect the surface morphology of different types of silicon wafer, busbars and grid fingers of solar cell. The first optical microscope used in this research is AmScope digital trinocular stereo microscope (Figure 3.5 (a)). The resolution capability of this microscope is poor. However busbars and grid finger analysis can be done with this microscope. The microscopes that are used to investigate the surface morphology of raw, saw damage removed and textured wafer are Micros Square, DS-600, Digital Microscope (U1000X) Model : TOL-00067 and ZEISS Stemi 508 microscope with axiocam 105 microscope camera (Figure 3.5 (b, c, d)). With all these microscopes the surface morphology of raw, saw damage removed can be well inspected however, Scanning Electron Microscope (SEM) is required to see the surface morphology of textured wafer.

(a)



(b)



(c) (d)

Figure 3.5 Different Optical Microscopes (a) AmScope Digital Trinocular Stereo Microscope (b) Micros Square, DS-600 (c) ZEISS Stemi 508 microscope with axiocam 105 microscope camera (d) USB Digital Microscope (U1000X) Model : TOL-00067

3.7 Four Point Probing *I-V* Measurement System

Four point probing current (I) – voltage (V) measurement system measures the sheet resistivity and sheet resistance of materials. The system measures sheet resistance and sheet resistivity by using the voltage and current readings from the four point probe. The sheet resistance and sheet resistivity follows the following relation:

$$\text{Sheet Resistance (Rs)} = \frac{\text{Sheet Resistivity}}{\text{Thickness}} \quad \ldots\ldots\ldots\ldots\ldots (2)$$

The unit of sheet resistivity is ohm-cm (Ω.cm). If Ω.cm is divided by the thickness of the material then sheet resistance is obtained. The unit of sheet resistance is ohm per square (Ω/□). Sheet resistance is determined when measuring the bulk or volume resistivity of thick or homogeneous materials such as bare silicon wafers or silicon ingots, using the four point probe technique [12]. Whereas Ω/□ is needed when measuring the resistance of a thin film of a material. This is because the thickness of thin film sometimes cannot be determined accurately thus Ω/□ is considered for thin film instead of Ω.cm. In this research work, Keithlink four point probing *I-V* measurement system [13] has been used to measure sheet resistance and sheet resistivity of the semiconductor materials (As shown in Figure 3.6). There are also several other four point probing *I-V* measurement system has been used for this research. However the accuracy of the Keithlink four point probing *I-V* measurement system is very good and it is an automated system that is why this system is broadly used in the research and its operational procedure is briefly discussed below.

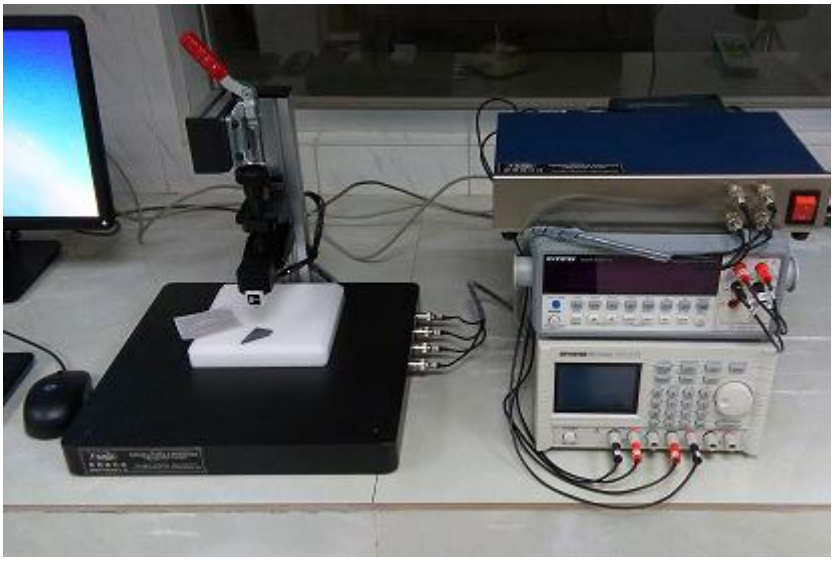


Figure 3.6 Keithlink Four Point Probing *I-V* Measurement System

Operational procedure of Keithlink four point probing *I-V* measurement system begins with turning ON all the system equipment's. They are the uninterruptible power supply (UPS), computer, the auto switch box for polarity change (blue box), dual measurement multimeter (GW Instek GDM-8261A) and programmable power supply (GW Instek PST-3202). After turning ON all the devices the sample is placed under the four point probe. To place the sample, the sample is first placed in the white board and directly under the four point probe. Then the round black knob turned so that the teeth (4 probe) are adjust just at the top of the sample. Then the red handle of four point porber is turned to the down position so that the four point probe (teeth) touches the sample. Next thing to do is to turn ON Kithlink IV measurement tool premium software. Now eneter the parameter values such as Meas. Point: 3 (Will measure three point per test), thickness: 200 μm (sample thickness), sample shape :(square/rectangle) and sample size. If sample size is not known then select user defined 4.532. Lastly running the simulation the sheet resistance, sheet resistivity values will be shown in the computer monitor.

3.8 Spectral Response Measurement System

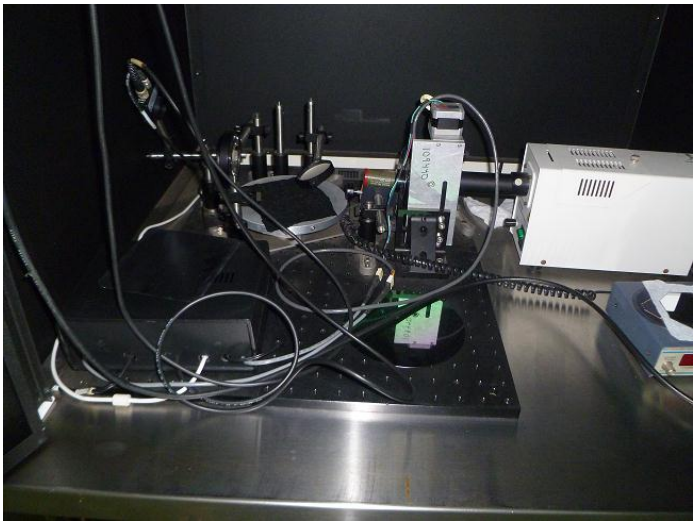


Figure 3.7 Inside View of Spectral Response Measurement System

The spectral response measurement system, as shown in Figure 3.7, is composed of a SR510 lock in amplifier (not visible in the picture), SR540 optical chopper, monochromator (400nm-1200nm), optical detector and lab view software. This system can measure the spectral response and relative reflectance of a material in the 400nm-1200nm range. Details of this system is discussed in the later chapter (chapter-8).

3.9 Wet Chemical Processing Bench

Solar cell fabrication requires wafer cleaning and texturing. This kind of processing requires wet chemical processing benches, exhaust, and water treatment system. In this research, Gratings Inc.'s wet chemical processing bench has been used (as shown in Figure 3.8). The exhaust system in the wet chemical processing bench drives away the fumes which is created during processing samples with chemicals. The samples are dried with the air-guns.

Figure 3.8 Wet Chemical Processing Bench

3.10 $POCL_3$ Diffusion Furnace

Phosphorus diffusion is used in the fabrication process for all *P*-type crystalline silicon wafers to form passivated, *N*-type emitter layer. Phosphorus diffusion is normally done using a liquid phosphorus tri-chloride ($POCl_3$) solution. At high temperature, the $POCl_3$ vapor decomposes to deposit phosphorous on silicon which is then diffused into silicon to form *P-N* junction. The $POCl_3$ diffusion furnace provides the option of phosphorus diffusion on *P*-type crystalline silicon wafers to from *N*-type layer using liquid $POCl_3$ solution. In this research, a $POCl_3$ diffusion furnace has been used. The $POCl_3$ diffusion furnace is actually an atmospheric pressure chemical vapor diffusion (APCVD) chamber. It operates at 1 atm pressure that's why it is also called an APCVD chamber. Although the system can operate at 1000°C phosphorus diffusion is done in the range of 850°C to 900°C. From the Figure 3.9 it seems that there are three diffusion chambers in the system. However the top most diffusion chamber is not operational. So the system includes two diffusion chambers, exhaust system, Gas piping system for nitrogen and oxygen gas, glass bubbler to hold liquid $POCl_3$ and atmospheric pressure gauge. Unfortunately the system does not include a flow meter. Thus accurate measurement of

gas flow rate into the diffusion chamber is difficult. The use of $POCl_3$ diffusion furnace for this research is discussed in later chapter (chapter-10).

Figure 3.9 $POCL_3$ Diffusion Furnace

3.11 Screen Printer

Screen printing is a process to print patterned metal contacts on the front and back surface of solar cells. Screen printing is done normally by an automated machine. Because of application of uniform pressure in the squeeze is difficult and accuracy is seriously required in case of screen printing process. Thus an automated screen printing system (Figure 3.10) is required and used in this work. However, in this work due to malfunction in the automated screen printing system only the vacuum chamber is operational and that part is only used. The vacuum chamber can only hold the wafer/sample nothing else. The application of metallic paste, squeeze pressure etc. all are done manually.

Figure 3.10 Screen Printer

3.12 Dryer Oven

(a) (b)

Figure 3.11 Dryer Oven (a) Closed (b) Open

To form metal contacts on solar cell screen printed pattern needs to be dried (baked) at a certain temperature for a fixed time. Normally the temperature is in between 100°c to 200°c. The drying is done in a Rio Grande dryer oven (Figure 3.11). Program can be set to reach the temperature to 120°c, 150°c or 200°c. If the temperature exceeds the set temperature then the dryer door is kept open to reduce the temperature.

3.13 Field Emission Scanning Electron Microscope (FESEM)

Field-emission microscopy (FEM) is an analytical technique used in materials science to investigate molecular surface structure and their electronic properties. Field emission scanning electron microscope (FESEM) is an instrument that provides topographical and elemental information at magnifications of 10 X to 300,000 X FESEM is a more powerful version of a scanning electron microscope (SEM) [14].

The main difference between a FESEM and a SEM lies in the electron generation system also known filed emission source [15]. There are two classes of emission source: thermionic emitter and field emitter. The thermionic emitters use electrical current to heat up a filament and the two most common materials used for filaments are Tungsten (W) and Lanthanun Hexaboride (LaB6). When the heat is enough to overcome the work function of the filament material, the electrons can escape from the material itself. Thermionic sources have relatively low brightness, evaporation of cathode material and thermal drift during operation. Field Emission is another way of generating electrons that avoids these problems. A Field Emission Gun (FEG); also called a cold cathode field emitter, does not heat the filament [16]. The emission is reached by placing the filament in a huge electrical potential gradient. The FEG is usually a wire of Tungsten (W). FESEM uses Field Emission Gun producing a cleaner image, less electrostatic distortions and spatial resolution < 2nm (that means 3 or 6 times better than SEM). In this research, a JEOL JSM-7600F FESEM has been used (Figure 3.12) to investigate the

surface morphology of different silicon samples. This FESEM can also perform Energy Dispersive Spectroscopy (EDS) measurement. So EDS measurement has also been done with this equipment.

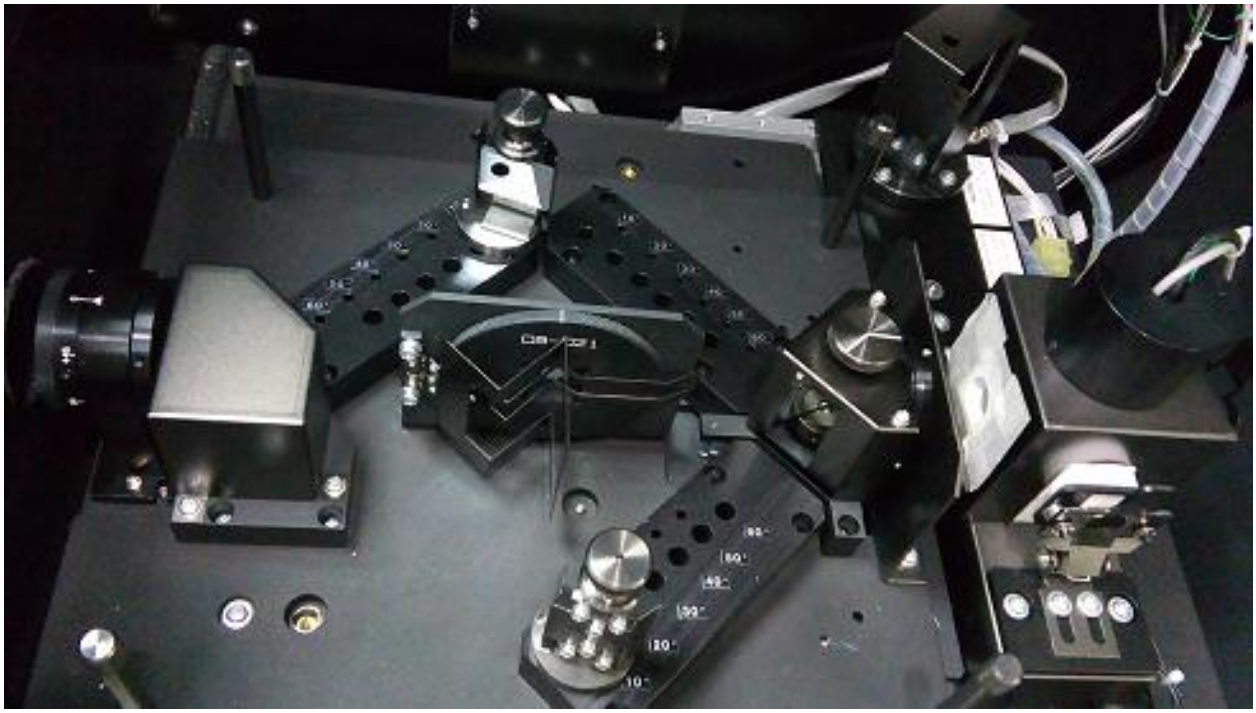
Figure 3.12 JEOL JSM-7600F FESEM

3.14 Ultraviolet-Visible-Near Infrared (UV-VIS-NIR) Spectrophotometer

A spectrophotometer is an instrument which measures the reflection or absorbance characteristics of a sample [17]. The spectrophotometer measures data and shows the graph of absorption/reflection versus wavelength which is also called the spectrum. An Ultraviolet-Visible-Near Infrared (UV-VIS-NIR) Spectrophotometer operates in the UV-VIS-NIR region and shows the particular graph for that region. The wavelengths for ultra-violet (uv), visible (vis) and near infra-red (nir) radiation are 10 to 400 nm, 400 to 780 mm and 780 to 3200 nm respectively [18]. Here in this research, a Hitachi UH4150 ultraviolet-visible-near infrared (UV-VIS-NIR) spectrophotometer has been used (Figure 3.13). The system uses a 60 mm high-sensitivity integrating sphere for reflectance measurement. The part number (P/N) is 1J1-0123. Spectralon® sphere coating is used in the integrating sphere [19]. The wavelength range of the integrating sphere is 190 nm - 2,600 nm. The system provide great accuracy because it measures absolute reflectance instead of relative reflectance using 'V-N' method. When the sample is not placed in the sample holder of UV-VIS-NIR Spectrophotometer, the system works in the 'N' configuration mode. In the 'N' configuration mode, base-line correction is done. After base-line correction, the sample is placed in the sample holder of UV-VIS-NIR Spectrophotometer and the system works in the 'V' configuration mode. That is the light is reflected from the sample in a 'V' path and falls on the photo detector. In this work, 250 nm - 840 nm wavelength range has been used.

The UV-VIS-NIR Spectrophotometer system has been broadly used in the research. The UV-VIS-NIR Spectrophotometer is situated at Institute of Fuel Research and Development Department, BCSIR, Dhaka. Thus its operational procedure is briefly discussed below.

(a)



(b)

Figure 3.13 Hitachi UH4150 ultraviolet-visible-near infrared (UV-VIS-NIR) spectrophotometer. (a) Outside View (b) Inside View

After turning ON the spectrophotometer machine and the computer, it is required to run the UV-Solution software. Once it is done, then base line correction of the system is required. To do that the mirrors must be placed opposite to each other and at same angles. Here, the mirrors

are placed at 10°. Furthermore the mirror in front of the detector must be turned in the clockwise direction so that the reflected light reaches the detector. No sample is placed at the round sample holder (placed in the middle of the system as shown in Figure 3.13 (b)). This is done because during base line correction the light travels in 'N' configuration from source to detector. The same light goes via another path directly from source to detector. The detector compares both light and if there are no sample in the sample holder then the system will show 100% reflectance and the wavelength vs. reflectance curve will be a straight line. Once the internal hardware arrangement is done, then 'Method' option is selected in the UV-Solution software home page. Then in the general tab 'wavelength scan' is selected. After that in the instrumentation tab the values of data mode, starting wavelength, end wavelength, scan speed, base line correction, attenuation and PMT mode & voltage values are given. For data mode reflectance (R%) has been selected. Starting and ending wavelength has been considered 840 nm to 250 nm. It is to be noted that wavelength changes occur in descending order. That is why, the starting wavelength is 840 nm and ending wavelength is 250 nm. Scan speed is considered 600 nm/min. The highest speed of the system is 1200 nm/min. Attenuation option is not enabled. Photo multiplier tube (PMT) mode is kept fixed and for that PMT voltage is considered 600 V. The PMT voltage can be increased or decreased. However, increasing PMT voltage like to 800 V not only will amplify the reflectivity but also the noise. If the PMT voltage is lowered than 600 V, then a condition may arise so that the detector will not be able to detect anything. Once all these parameters are selected in the instrumentation tab, lastly base line correction has been selected to 'system'. Now at the home page of UV-Solution software base line operation has been activated to calibrate the system. Once the base line calibration is done, sample is placed in the sample holder for measuring reflectivity. Before reflectivity measurement, the mirror position in front of the sample must be changed. Both the mirrors angle must be same (here it is kept at 10°) and the arrangement should be in the 'V' configuration. Also the mirror, in front of the detector, must be turned in the counter clockwise direction so that the reflected light reaches the detector. Once it is done, now at the home page of UV-Solution software measurement option has been activated to measure the reflectance data of the sample.

3.15 Conveyor Belt furnace

A conveyor belt furnace is a furnace that uses a conveyor belt to carry process parts or material through a heating chamber for rapid thermal processing. It is designed for fast drying and curing of products and is nowadays widely used in the firing process of thick film and metallization process of solar cell manufacturing. Other names for conveyor belt furnace include metallization furnace, belt furnace, fast fire furnace etc.

After screen printing process, electrical contacts are not formed permanently. To do that co-firing is required to form permanent contact on solar cell and the process is known as metallization process. The co-firing is done using a conveyor belt furnace. Here a Radiant Technology Corp. (RTC) conveyor belt furnace (provided by Gratings, Inc.) has been used (Figure 3.14). Unfortunately one of the problem of this furnace is it does not have the option to provide nitrogen and oxygen gas that is required for metallization process.

Depending on model a conveyor furnace can have maximum five sections. They are pre-heating section, binder burn out section, heating section, firing section and cooling section. However, the RTC furnace does not have the Pre-heating section. The pre-heating has been done in the dryer at 100-150 °C for 10–15 minutes to remove solvents. The firing has been done in the conveyor belt furnaces at temperatures between 500-1000 °C.

Figure 3.14 Radiant Technology Corp. (RTC) Conveyor Belt Furnace

3.16 LIV tester

The Light intensity Current Voltage (*LIV*) tester is used to measure the efficiency of solar cell. The solar cell *LIV* measurement system also determines fundamental device parameters including short circuit current (I_{sc}), open circuit voltage (V_{oc}), fill factor (*FF*), and maximum power (P_{max}). To measure the efficiency the system has to be calibrated by using a calibrated solar cell (The calibrated solar cell is a solar cell, whose efficiency is known and is used for calibrating the *LIV* tester). Unfortunately the calibrated cell being broken the system measurement has been done without calibration. So the data accuracy of the system is questionable.

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Chapter 4

FABRICATION PROCESS OF MONOCRYSTALLINE SILICON SOLAR CELL

4.1 Introduction

Since the fabrication of the first GaAs solar cell in 1956, with an efficiency of 4%, a steady effort to improve the efficiency of the cells has been undertaken and so far efficiencies in the range of 20-30% has been achieved. Bangladesh, being a tropical country, undergoes an average daily irradiation is 5 kWh/m^2/day. Taking these advantageous situation, already more than 4.5 million solar home systems (SHSs), 3 solar mini grids and about 671 solar irrigation systems have been established in Bangladesh. So far, there is a huge demand of solar panel in the remote area of Bangladesh. However, in Bangladesh solar cell is still not fabricated commercially.

For the first time in 2015, monocrystalline silicon solar cell has been fabricated at one and only monocrystalline solar cell fabrication laboratory available in Atomic Energy Research Establishment, Savar, Bangladesh. The fabricated silicon solar cells in this laboratory have the efficiency of only 6.89% so far. There are several ways that a monocrystalline solar cell can be fabricated like standard solar cell fabrication process, buried contact solar cell, bi-facial cell, Passivated Emitter Rear Contact (PERC) solar cell etc. This chapter discusses about the fabrication process of monocrystalline silicon solar cell in Bangladesh.

4.2 Fabrication steps of mono-crystalline silicon solar cell

The majority of silicon solar cell production is currently based upon a very standardized process which is forming a P-N junction [1]. The fabrication process ofnine silicon wafer with an area of 150×150 mm^2. The pseudo-square silicon wafers are show in Figure 4.1.

Cutting silicon into wafers leaves the surface covered with cutting dust, particles, waste, organic compound, ionic compound etc. and the surface is damaged due to the action of the sawing. For this reason, wafers are needed to be cleaned in a hot chemical solution to remove the surface contamination. The cleaning process can also be done using saw damage removal process. Moreover, after saw damage removal process texturing on solar cell is done to reduce reflection and enhance light absorption [2-3].

After cleaning and texturing, the edge isolation process is done to remove the *P-N* junction short circuit. Edge isolation is done by using an edge isolation barrier paste. Next, *N*-type layer is formed on a P-type silicon wafer using phosphorus diffusion technique in diffusion chamber [4].

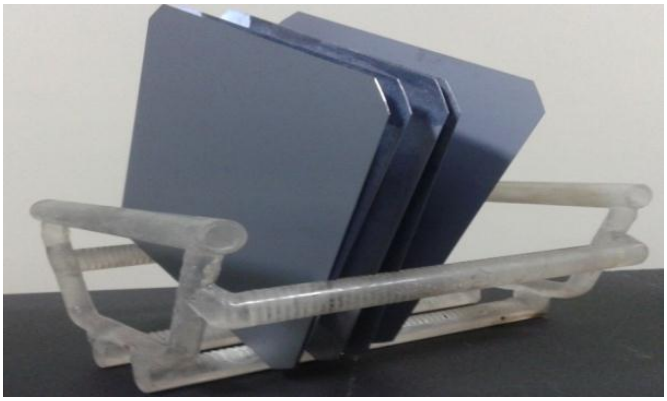


Figure 4.1 *P*-Type Mono-Crystalline Silicon Wafers

After formation of *P*-*N* junction, metallization process is necessary for creating output contact terminals. At front surface of solar cell silver and at the back surface aluminum busbars and fingers has been screen printed. Afterwards, the silver and aluminum busbars and fingers along with solar cell are heated at very high temperature in a conveyer belt furnace, for the formation of contact.

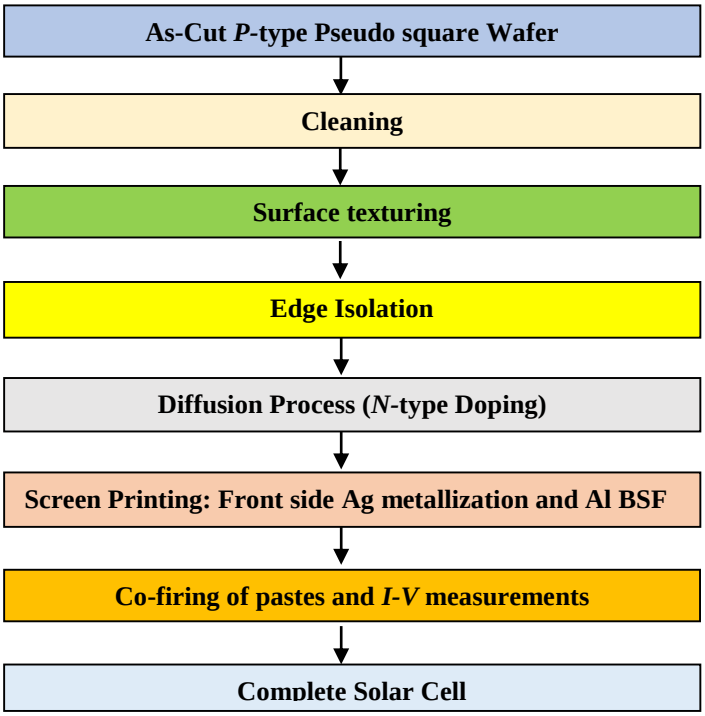


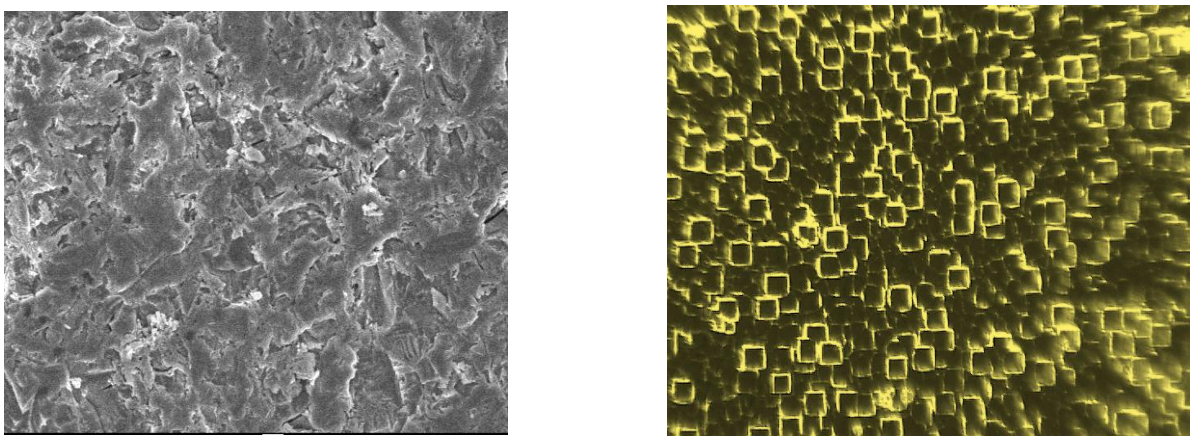
Figure 4.2 Fabrication Steps of Mono-Crystalline Solar Cell in Bangladesh

Figure 2 illustrates the mono-crystalline solar cell fabrication process used in Bangladesh. All the steps involved in fabrication of solar cell in Bangladesh are elaborately discussed in the following sections of this chapter.

4.3 Cleaning Process

Cleaning of Si wafer is essential in order to remove unwanted particles including metallic impurities, residues [5]. In Bangladesh, raw wafer cleaning process are done in two steps. In the first step, sodium hydroxide (NaOH) and DI water (H_2O) are used for cleaning. By adding

600gm NaOH pellet with 6 liters of DI water in a clean breaker, 10% NaOH solution has been made in the laboratory. To remove the organic contaminates from silicon wafer, the silicon wafer has been dipped into 10% NaOH solution at 70°C for about 10 minutes. Then the wafers are dipped into hydrofluoric acid (HF) solution for 3 minutes in order to remove native oxide layer. The ratio of hydrofluoric acid is HF: H_2O at 1 ml: 50 ml.

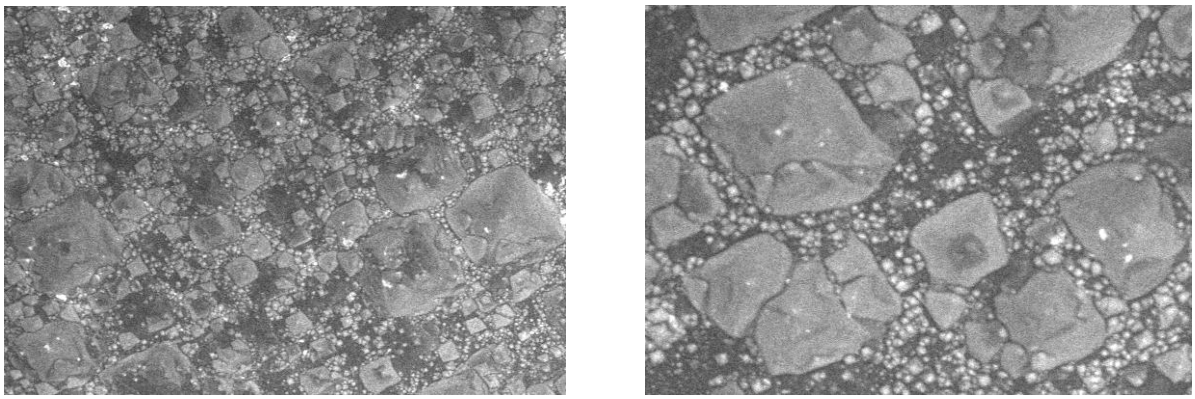


(a) (b)

Figure 4.3 (a) Saw Damaged Silicon Wafer Surface (b) Saw Damage Removed Silicon Wafer Surface

4.4 Texturing Process

After saw damage removal process texturing on solar cell is done to reduce reflection and enhance light absorption [2-3]. In addition, surface texturing scatters light inside the semiconductor in order to trap it inside the wafer and thus increases efficiency of the solar cell. For texturing process alkaline-based chemical are used in Bangladesh. The alkaline-based chemical solution has been made by using KOH, IPA and DI-water solution. The ratio of KOH (Potassium Hydroxide): IPA (Isopropyl Alcohol): H_2O (DI-water) are 1 gram: 5 ml: 125 ml. The wafers are dipped into the solution and heated at 70^0C for 10 minutes. After 10 minutes pyramid structure is formed upon the surface of the wafer. Figure 4.4 shows the SEM images of textured surface of *P*-type silicon wafer.



(a) (b)

Figure 4.4 SEM Images of Textured Silicon Wafer (a) 2000 Times Magnification (b) 5000 Times Magnification

4.4.1 Reflection of textured surface and raw surface

The variation of reflectance has been observed using spectral response measurement system. From the measurements, it is seen that, the average reflectance for the surface of raw silicon wafer between the wavelength 675 to 1075 nm is 5.337619 Arbitrary Unit (AU) and for the same wavelength range the average reflectance of textured silicon wafer is 3.763397 AU (Figure 4.5). The difference of average reflectance between raw wafer and textured wafer is 1.614222 AU. It is also seen from the graph that the raw wafer surface reflectance is significantly higher than the textured wafer and maximum 30.40% surface reflectance is observed at 975 nm.

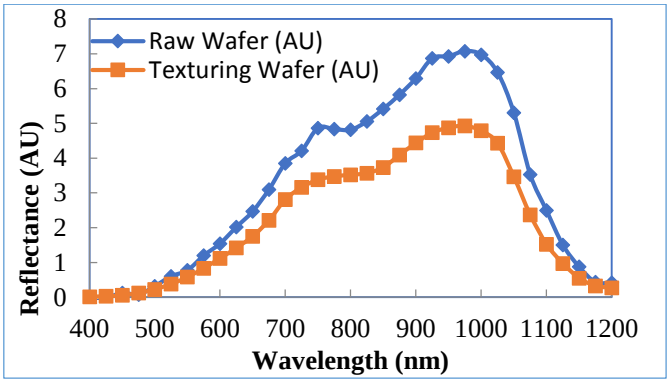


Figure 4.5 Spectral Reflection Measurement Data of Raw Silicon Wafer and Textured Wafer

4.5 Edge Isolation

Edge isolation is a process that removes the phosphorous diffused area around the edge of the *P*-type wafer, so that the *N*-type layer is isolated from the *P*-type layer [6]. During phosphorus diffusion the edge of the *P*-type wafer becomes *N*-type thus acts as short for *P*-*N* junction of the solar cell and thus reduces the efficiency of solar cell. So edge isolation is absolutely necessary. Here, in Bangladesh for the edge isolation process, edge isolation paste is used before phosphorous diffusion.

After wafer cleaning and texturing process, the sides of the wafers are covered with edge isolation paste by a screen printing machine. Then the wafers are dried for 10 minutes in a preheated oven at 200 °C.

4.6 Diffusion Process

There are many ways to form *N*-type layer on *P*-type layer such as epitaxial growth, ion implantation, and diffusion [7]. In diffusion process, Phosphorus Oxychloride ($POCl_3$), Oxygen (O_2) and Nitrogen (N_2) gases are widely used to create *N*-type layer upon *P*-type silicon wafers. [8-9]. In Bangladesh, for diffusion $POCl_3$, N_2 and O_2 gases has been used. The whole process is carried out in diffusion chamber at 850-900^{0}C. As $POCl_3$ has a boiling temperature of 105.8 °C [10], it decomposes into P_2O_5 and reacts with O_2, thus creating phosphosilicate glass (PSG) [SiO2:P2O5)x] layer upon silicon surface. After formation of PSG-Si interface, the phosphorus atoms penetrate through the Si-wafer and diffusion happens [7].The following reactions take place during diffusion process:

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2$$

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2$$

$$P + 3Si \rightarrow N\text{-type dope Si}$$

4.7 Screen Printing Process

Screen printing process is most commonly used to print metal contacts on back and front surfaces of solar cells. In front surface (*N*-type) Silver paste is used, whereas in back surface (*P*-type) aluminum paste is used in screen printing process. Aluminum contact on the wafer backside also serves by forming a heavily diffused p++ layer that reduces contact resistance and creates back surface field.

4.8 Co-Firing Process

A conveyer belt furnace has been used to form permanent contacts by heating the screen printed contacts on silicon solar cells. Rapid thermal annealing is important because it forms low-resistance ohmic contacts and provides proper contact between the conductor and the semiconductor of solar cell. In fabricating solar cells in Bangladesh, the temperature zones of conveyer belt furnace are 500°C, 600°C and 800 °C respectively. Figure 4.6 shows initial process of contact firing of solar cell in conveyer belt furnace.

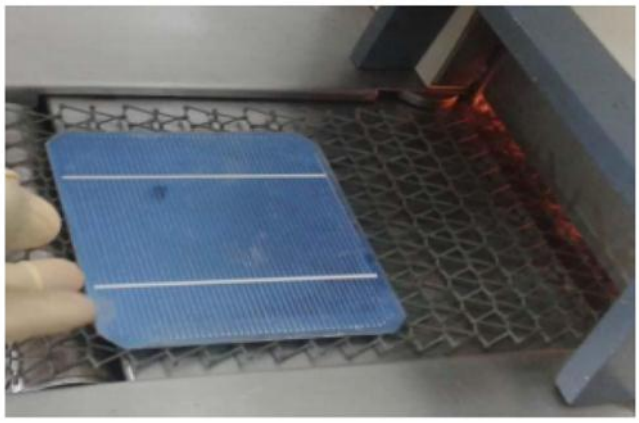
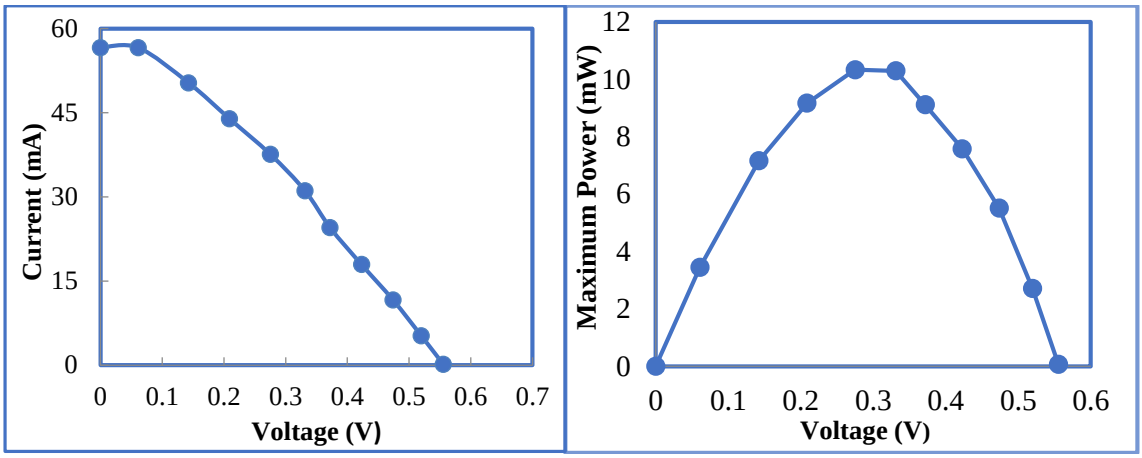


Figure 4.6 Initial Process Contact Firing of Solar Cell in Conveyer Belt Furnace

4.9 Results and Discussion

The Light intensity, Current and Voltage (*LIV*) test, which is also known as *LIV* test, determines the efficiency of a solar cell. It also determines the open circuit voltage (V_{oc}), short circuit current (I_{sc}), maximum power (P_{max}) and fill factor (*FF*). Xenon-arc lamp has been used in *LIV* testing as it is much closer to sunlight spectrum. *LIV* data are shown in Figure 4.7, where the light intensity has been 150mW/cm^2, with active surface area 161cm^2, and cell thickness of 200μm.

From the *LIV* test, labview software provides *I-V* curve of the locally fabricated solar cell. The following results has been found in case of the fabricated monocrystalline silicon solar cell in Bangladesh. The value of maximum power (P_{max}), maximum voltage (V_{max}), maximum current (I_{max}), short circuit current is (I_{sc}) and open circuit voltage (V_{oc}) respectively are 10.3369 mW, 0.27504V, 37.5833mA, 56.5867mA and 0.555462V.



(a) (b)

Figure 4.7 *LIV* Measurement Data of a Locally Fabricated Solar Cell (a) Current-Voltage curve (b) P_{max}-V curve

Fill factor (FF):

$FF = V_m I_m / V_{oc} I_{sc}$

= 0.328868

Efficiency (η):

$\eta = P_{out} / P_{in}$

$= [(V_{oc} I_{sc} \times FF) / P_{in}] \times 100\%$

$= 6.89\%$. $[P_{in} = 150 mW/cm^2]$

The efficiency of the locally fabricated solar cell is 6.89%.

4.10 Summary

In summary, the fabrication steps of monocrystalline silicon solar cell has been discussed in this chapter. The first fabrication of monocrystalline silicon solar cell has been done in Bangladesh Atomic Energy Commission (BAEC) and the efficiency of solar cell is currently 6.89%. It is seen that, it is less efficient than the commercially available solar cell in the market. Now, the main challenge is to find out the reasons for achieving such low efficiency and to find the remedies to increase the efficiency of the locally fabricated solar cell.

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Chapter 5

PROBLEM IDENTIFICATION OF THE FABRICATED MONOCRYSTALLINE SILICON SOLAR CELL IN BANGLADESH

5.1 Introduction

On the 22nd of April 2016, Bangladesh signed the Paris agreement [1], whose main goal is to reduce greenhouse gas emission and keeping global warming well below 2° Celsius [2]. Moreover, to ensure planetary habitability for today's and future generations the whole world is making steps to achieve 100 % renewable energy [3]. To go along with all these issues, in 2015 solar cell (with efficiency 6.89%) has been fabricated in Bangladesh for the first time [4]. But the efficiency of the fabricated solar cell is lower than commercially available solar cells, this chapter discusses about the problem analysis of monocrystalline silicon solar cell fabricated in Bangladesh. It is expected that after finding the problems, appropriate measures can be adopted to improve the efficiency of solar cell.

5.2 Problem Identification

5.2.1 Clean Room

Modern solar cell manufacturing is performed in a sophisticated facility known as a clean room. A clean room is a facility that is isolated from outside environment and free from pollutants such as particles, metals, organic molecules, electrostatic discharge (ESD) and chemical vapors [5]. A typical room in urban environment contains 35,200,000 particles per cubic meter (Size range of 0.5 μm and larger in diameter) and known as ISO 9 cleanroom, where as an ISO 1 cleanroom has no particles in that size range and only 2 particles per cubic meter of size 0.2 μm and smaller [6]. U.S. General Service Administration's standard (also known as FS209E) class 100 to 1000, equivalent to International Standards Organization (ISO) ISO 5 – ISO 6 class requirement has been not meet during the solar cell fabrication in Bangladesh. By using met one a2400 laser particle counter it is seen that ISO class is in between ISO 7 and ISO 8.

5.2.2 Wafer Selection

The first step of making silicon solar cell is choosing the *P*-type silicon wafer. For single crystalline silicon solar cell there are two ways that *P*-type silicon wafer can be manufactured. They are of Czochralski (CZ) method and Float Zone (FZ) method and the wafers are called CZ silicon wafers and FZ silicon wafer. It is seen that in FZ silicon wafer, oxygen is less than 10^{16} atom/cm^3 where as in Grade A type CZ wafer it is 9×10^{17} atom/cm^3. Also carbon concentration is less than below 10^{16} atom/cm^3 in FZ where as in CZ, it is 1×10^{17} atom/cm^3 [7]. These oxygen and carbon are the main impurities of solar cell processing and the precipitation of oxygen and carbon occurs during crystal growth [8]. Moreover, oxygen defects reduce the lifetime of the bulk. Since the melt does not come into contact with a quartz crucible, and no

hot graphite container is used during FZ crystal growth, FZ wafer has lower oxygen and carbon concentration compared to CZ silicon [9]. In fact FZ wafer is superior over CZ wafer is based on low impurity, minority carrier bulk lifetime and low resistivity variation. Despite the advantages of FZ wafers, CZ wafer has been used in Bangladesh.

5.2.3 Edge Isolation

Edge isolation is a process that removes the phosphorous diffused area around the *P*-type wafer, so that the front emitter (*N*-type layer) is isolated from the rear (*P*-type layer) [10]. The removal diffused layer around the edge of the solar cell is absolutely necessary because the diffused layer acts as short for *P-N* junction of the solar cell and thus reduces the efficiency of solar cell. Here in Bangladesh, for the edge isolation process, edge isolation paste has been used before phosphorous diffusion. Little is known about the edge isolation paste which has been bought from the market and it is assumed as one kind of flux rosin. Using edge isolation paste is one of the main reason for achieving low efficiency solar cell in Bangladesh. But for better performance in the edge isolation process it is proposed to use Microwave Plasma System [11]. Where edge isolation is done by stacking the wafers on top of each other and generating plasma with microwave frequency 2.45 GHz and having an etching environment consists of combination of fluorinated gas (CF_4) and oxidant gas (O_2).

5.2.4 Shunt Resistance

Significant power loss can be seen in solar cell due to low shunt resistance (R_{SH}) as shown in Figure 5.1. For an ideal cell, R_{SH} should be infinite and should not provide an alternate path for current to flow. If R_{SH} is low then the value of V_{oc} will also be low. In the locally fabricated solar cell shunt resistance is found low.

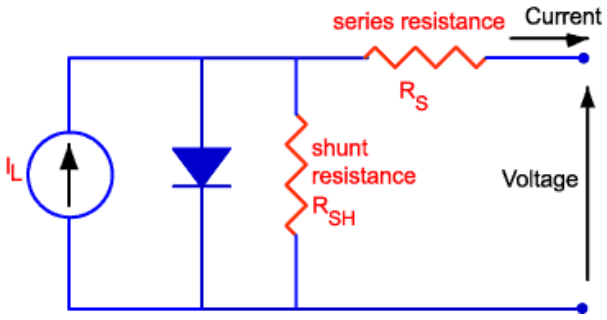


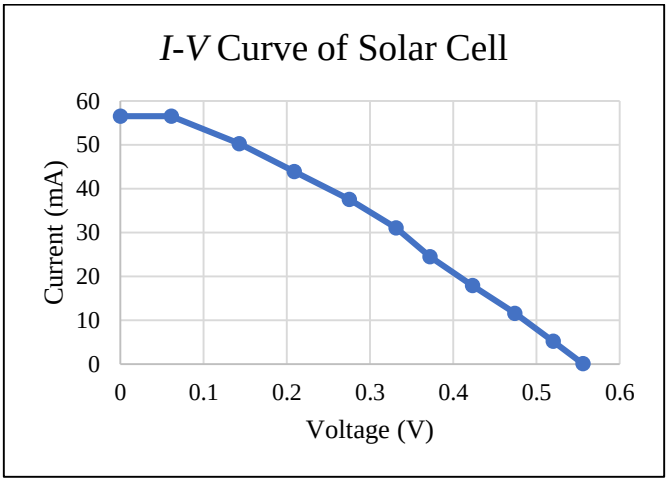
Figure 5.1 Shunt Resistance

Under low light conditions the shunt resistance of the locally fabricated 12.5×12.5 cm^2 solar cell is 234 ohm. Whereas good solar cell has more than 1000 ohm of shunt resistance [12].

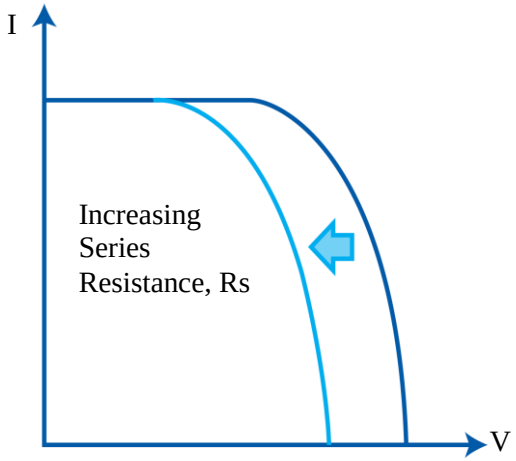
5.2.5 Series Resistance

The Light intensity Current Voltage *(LIV)* measurement instrument has been used to measure the current and voltage of the fabricated solar cell. After obtaining the current voltage data the *I-V* characteristics curve has been drawn, as shown in the Figure 5.2(a), and by using two-curve method [13] (which uses the following series resistance equation) the series resistance of the fabricated solar cell has been determined.

$$\mathbf{Rs} = \frac{\Delta V}{\Delta I} = \frac{V_1 - V_2}{I_2 - I_1}$$



(a)



(b)

Figure 5.2 *I-V* Curves of Solar Cell: (a) Fabricated Solar Cell (b) Ideal Solar Cell Showing the Effect of Increased Series Resistance [14]

The series resistance, Rs of the fabricated solar cell is 6.197 Ω.cm^2. Which is much higher compared to the high efficient solar cell series resistance value, that varies from 0.3 Ω.cm^2 to 1 Ω.cm^2 [15]. The high series resistance of the fabricated solar cell can also be seen from the *I-V* curve. From Figure 5.2 (b) it is seen that, due to the large series resistance the *I-V* curve of the fabricated solar cell deviates from the ideal *I-V* curve of the solar cell shown in.

5.2.6 Minority Carrier Diffusion Length & Minority Carrier Life Time

Light-induced surface photo voltage (SPV) measurement system is used to measure the minority carrier diffusion length. It is seen that minority carrier diffusion length is 88 µm which lacks the required diffusion length because typical minority carrier diffusion length is 100-300 µm [16].

Measurement of minority carrier life time is also done using the following equation.

$L = \sqrt{D\tau}$

Where, L is the diffusion length in meters, D is the diffusivity in m^2/s and τ is the lifetime in seconds. The standard value diffusivity is considered as 27 cm^2 /s and from the equation it is found that the minority carrier life time is 2.8681 µsec, which is much below 10 µsec.

5.2.7 Anti-Reflection Coating (ARC) Layer

Although, anti-reflection coating (ARC) layer reduces reflection and increases efficiency of solar cell, no anti-reflection coating layer has been applied in the fabricated solar cell in the research Laboratory of Atomic Energy Research Establishment (AERE), Savar, Bangladesh.

5.2.8 Wafer bowing

Wafer bowing is bending of solar cell. The wafer bows and forms a convex or concave shape instead of flat surface when heating in the RTA (Rapid Thermal Annealing) furnace or when cooling the solar cell after metallization process [17]. Wafer bowing has a direct impact on the efficiency of solar cell [18]. So one of the most critical processing steps is firing process (metallization process) where wafer bowing may happen. Although there are a number of factors that can affect the shape of a monocrystalline silicon wafer, here wafer being thin (wafer thickness is 200 µm), and external influences like improper temperature during metallization process are the main reasons for the wafer to become concave or convex [19]. Wafer bowing has been observed in the solar cell fabricated in Bangladesh as shown in Figure 5.3.

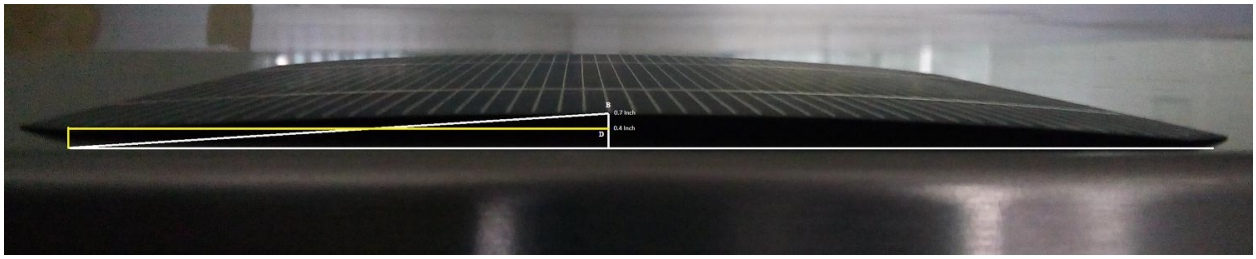


Figure 5.3 Bowed Solar Cell

Height increase of bowed solar cell has been measured from Figures 5.3 and 5.4

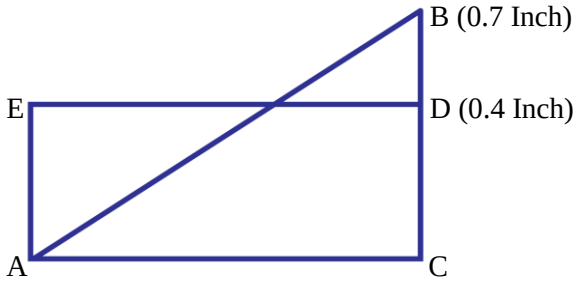


Figure 5.4 Measurement of Increased Height

In Figure 5.3, the peak height of the bowed wafer is denoted as Point B and from the Point B a straight line is drawn to the ground (Point C). From the image, distance from peak point B to the ground (Point C) has been measured and the measured value is 0.7 inch as shown in Figure 5.4. Again, Point D represents peak point of a solar cell which is not bowed. Measurement shows the distance from peak Point D to the ground is 0.4 inch. The distance between point B and Point D is 0.3 inch, which indicates the increase in height of bowed solar cell. Now, by

using a dial indicator experimentally the peak height D of the solar cell has been measured, which is 180 µm. So, the image equivalent point D height 0.4 inch is actually equal to 180 µm. That means actual increased height by bowing of solar cell is 135 µm and peak height of the bowed wafer (point B) is 315 µm. The calculated angles are 4°, 86° and 90°.

5.2.9 Micro-cracks in busbars

A micro-crack is microscopic crack in a material. Micro cracks increase mechanical wafer breakage [20] and micro cracks in busbars and grid fingers hinder electric current flow thus reducing the power and efficiency [21].

Various methods like scanning acoustic microscopy, resonance ultrasonic vibration (RUV), optical microscopy are used to detect micro cracks in solar cell [22]. As optical microscope is easy and non-destructive technique, it has been used to determine the micro cracks of locally fabricated solar cells. Figure 5.5 shows micro cracks in busbars in the tested solar cell. Presence of micro cracks in busbars are one of the reasons that results in low efficiency.

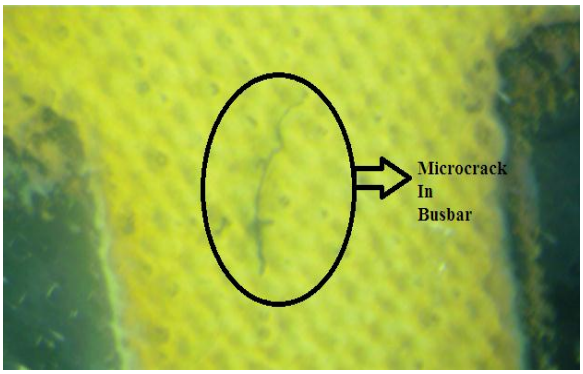


Figure 5.5 Micro Crack in Busbar of Locally Fabricated Solar Cell

5.2.10 Busbars and Grid-Fingers

Metallic top contacts are essential for collecting the current generated by a solar cell. The metallic top contacts having larger width are called busbars.

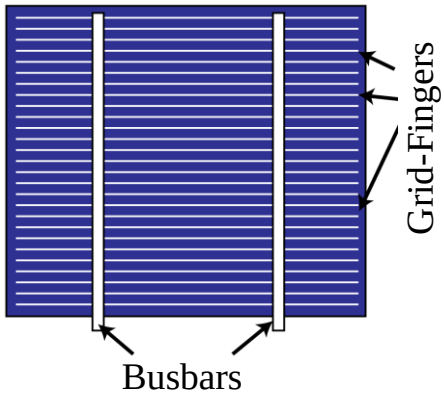


Figure 5.6 Busbars and Grid-Fingers

The external wires are directly connected to the busbars. In addition to busbars, the narrow lines of metallization which are perpendicular to the busbars are called grid fingers. The grid fingers are thinner than busbars and collect the photo generated current from the cell and supply to the busbars [23]. Both busbars and grid fingers are shown in Figure 5.6.

5.2.10.1 Optical analysis

Busbars and fingers are supposed to be straight and of uniform width and height. Unevenness of busbars and grid fingers increases series resistance and reduces the power and efficiency. A standard commercial solar cell (provided by Gratings Inc. [24]) busbars and grid-fingers uniformity has been analyzed using optical microscope. The shape of the busbars edge and grid-finger of this cell is shown in Figure 5.7 and Figure 5.8.

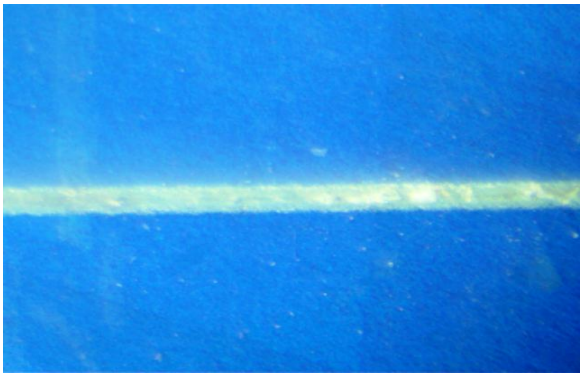


Figure 5.7 Grid-finger of Commercial Solar Cell

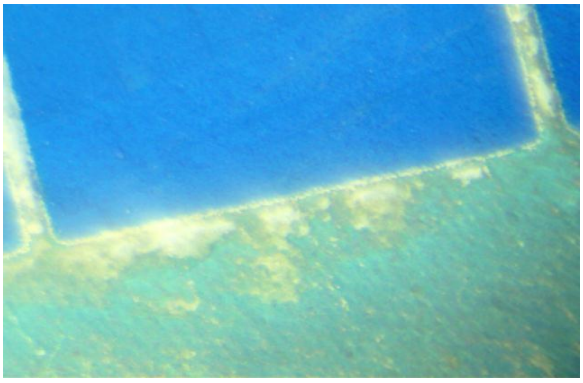


Figure 5.8 Busbar Edge of Commercial Solar Cell

Figure 5.9 Busbar of Indian Cell

Figures 5.7 and 5.8 show that busbars and grid fingers are uniform and straightforward. Magnifying more, comparing busbars between an commercial solar cell and an Indian solar cell (Tata BP Solar Ltd.[25]) it is seen that the silver paste are less dispersed and more straight

in the commercial solar cell than the Indian cell. The busbar of commercial solar cell and Indian cell are shown in the Figure 5.9 and Figure 5.10 respectively.

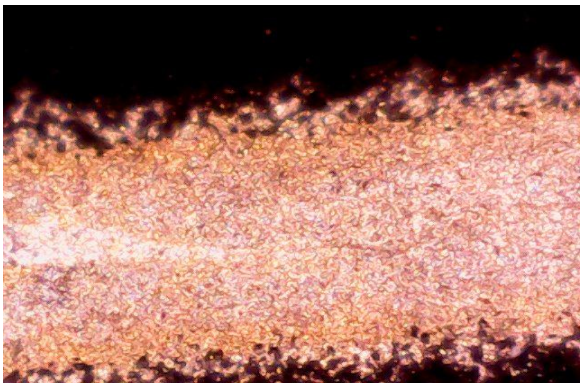


Figure 5.10 Busbar of Indian Cell

Upon inspection of the Busbar edge of a solar cell fabricated in Bangladesh, highest silver paste disperse is seen as shown in Figure 5.11.

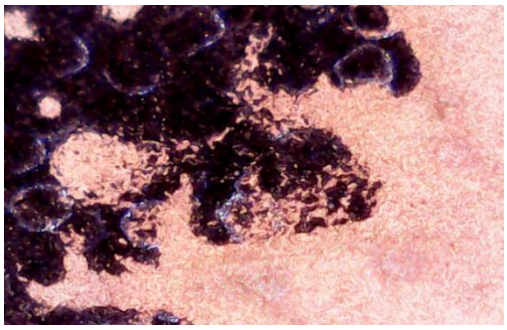


Figure 5.11 Busbar Showing Dispersed Silver Paste in the Solar Cell Fabricated in Bangladesh

The grid-fingers of the solar cell fabricated in Bangladesh are less straight forward and in some places degenerate silver paste has been seen as shown in the Figure 5.12 and Figure 5.13.

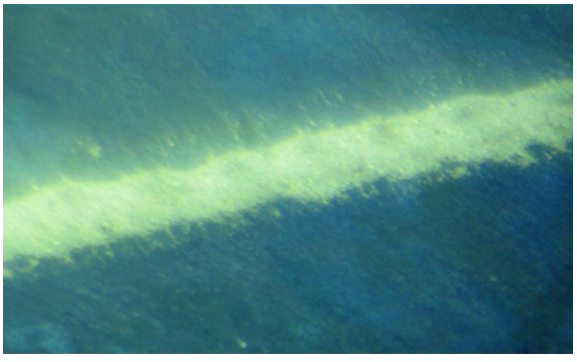


Figure 5.12 Less Straight Forward Busbar

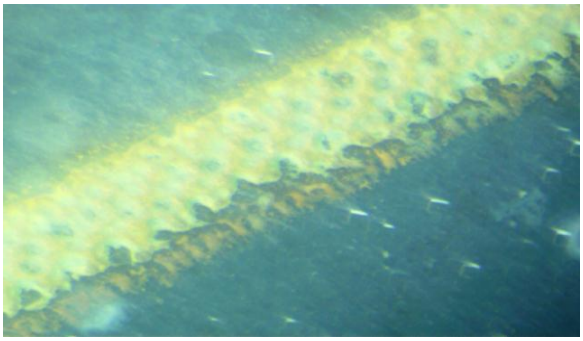


Figure 5.13 Degenerate Silver Paste in Grid- Fingers of Solar Cell Fabricated in Bangladesh

5.2.10.2 Surface profile analysis

Surface profilometer or surface profiling system is an instrument used to measure the roughness of a surface [26]. In a surface profiling system a stylus run along the sample surface and the up-and-down movements of the stylus are measured. Here a Dektak 150 Surface Profiling System has been used to measure the grid- fingers surface height uniformity.

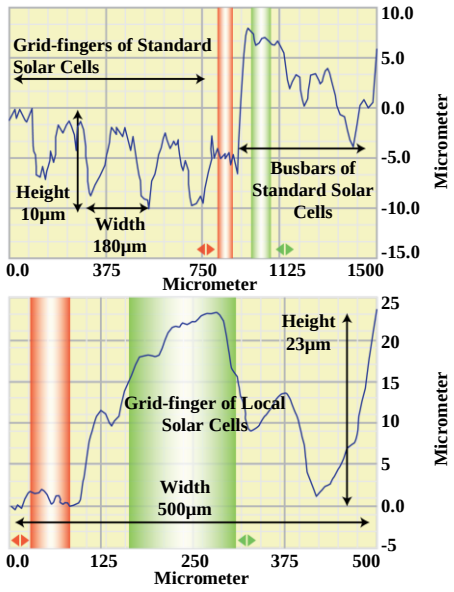


Figure 5.14 Grid-fingers of Standard and Local Solar Cells Showing Height, Width and Uniformity

In the upper part of Figure 5.14 shows Dektak 150 data of the standard solar cell grid-fingers, whereas the lower part of the Figure 5.14 shows the grid-fingers of the locally made solar cell. Also, the X-axis rand Y-axis represents the distance and height in micrometers in the Figure 5.14. From Figure 5.14, it is seen that the standard solar cell grid-fingers are a lot thinner in width than locally made solar cell. Measurement shows the maximum height of the standard solar cell grid-fingers are 10 µm.

Moreover, the width of grid-fingers are 180 micrometer and aspect ratio which is defined as the height to width ratio (shown in Figure 5.15) is 0.0556 for the standard solar cell. On the other hand, again from Figure 5.14 it is seen that maximum height of the grid-fingers are 23 µm, width is 500 µm and aspect ratio is 0.046 µm for locally made solar cell.

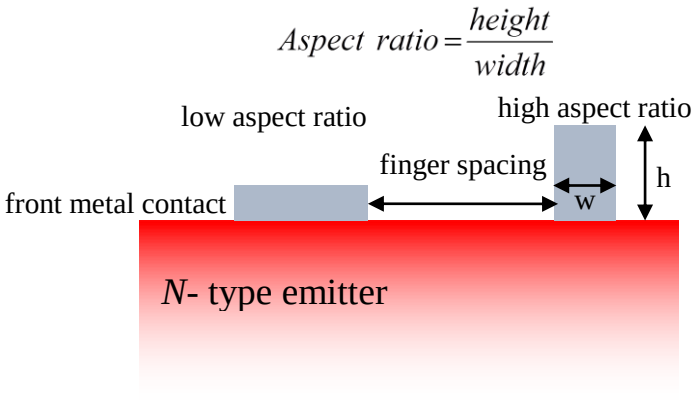


Figure 5.15 Aspect Ratio

High aspect ratio is required for better efficiency [27], although from the obtained data, it is clearly seen that locally made solar cell aspect ratio is little bit lower than the standard solar cell.

Busbars of both locally made and standard solar cells surface has been analyzed to determine the surface uniformity. It is seen that more hills and valleys exits in locally made solar cell, maximum 23 µm variation is observed whereas 8 µm variation is observed in the standard solar cell as shown in Figure 5.16.

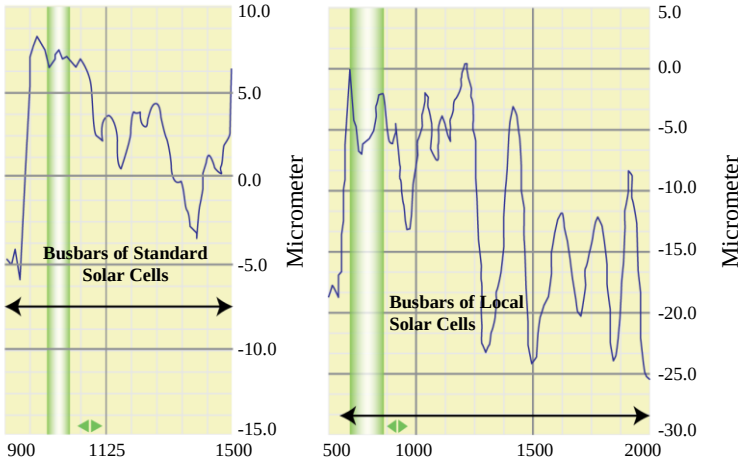


Figure 5.16 Busbars of standard and local solar cells showing height, width and uniformity

It confirms the lacking and degeneration of silver paste in busbars observed using optical microscope analysis as shown in the Figure 5.11.

5.2.11 Metallization problem

Metallization is a very important step for solar cell fabrication because it strongly affects the efficiency of solar cell. If optimum temperature and environment is not met in the conveyer belt furnace during metallization process cracks formation, bending of the wafer, high series resistance, low shunt resistance etc. are produced and that leads to an increase in leakage current therefore performance of the solar cell is deteriorated.

From *I-V* curve of locally fabricated solar cell high series resistance (6.197 Ω.cm^2) and low shunt resistance (234 Ω) has been observed. Wafer bowing and micro-cracks are also observed and has been discussed earlier in this paper. The reasons for these circumstances are: during

metallization process no oxygen and nitrogen gas has been used in the conveyer belt furnace, moreover conveyer belt furnace has no option for providing O_2 and N_2 gas [28].

5.2.12 Doping concentration of *P*-type wafer

P-type wafers with various doping concentration are found in today's world market, for different application like, IC fabrication, solar cell fabrication etc. have been in Bangladesh, Rene-Sola *P*-type, as-cut, monocrystalline silicon wafers has been used to fabricate solar cell. Specification says that sheet resistance of *P*-type as-cut monocrystalline silicon should be within 1-3 Ω-cm. However, from four point probe measurement it is seen that the sheet resistance lies between 1.03 Ω-cm to 9.79 Ω-cm. So greater variation in sheet resistance is observed and it is very difficult to take an average sheet resistance. The sheet resistance varies due to the variation of doping concentration of *P*-type wafer. Using PC1D simulation software it is seen that for the sheet resistance of 1.03 Ω-cm to 9.79 Ω-cm, doping concentration varies from 1.465×10^{16} cm^{-3} to 1.398×10^{15} cm^{-3}. For high efficiency solar cell *P*-type wafers sheet resistance is 0.1 Ω-cm to 0.5 Ω-cm [29]. That is doping concentration lies between 2.341×10^{17} cm^{-3} to 3.255×10^{16} cm^{-3}. So the *P*-type wafers used during fabrication of the local cell, its doping concentration is lower than high efficient solar cell. Moreover, 0.1 Ω-cm to 0.2 Ω-cm type wafer are commercially found but these type of wafers are not used during solar cell fabrication in Bangladesh.

5.2.13 Silver and Aluminium paste

Expired silver and aluminium paste has been used during solar cell fabrication in Bangladesh (Figure 5.17). Later both silver and aluminium paste have been bought from Suzhou Kaiyuan Minsheng Sci & Tech Corp. Ltd. However, the silver and aluminium content is low compared to the standard solar cell. Here the silver and aluminium content is 45-60%, 60-80%, respectively. Whereas in general silver and aluminium content is 80-90%, 70-80%, respectively [30-31].

Figure 5.17 Expired Silver and Aluminium Paste

5.3 Summary

In this chapter, problems of locally made monocrystalline silicon solar cell has been discussed. Use of edge isolation barrier paste is one of the main reason for achieving low efficiency. Problems are found in clean room, CZ (Czochralski) wafer, low shunt resistance, high series

resistance, edge isolation, Minority carrier diffusion length and anti-reflection coating (ARC) layer. Problems like wafer bowing, micro-cracks in busbars, dispersed and degenerated silver paste in busbars, no straight and smooth grid-fingers and busbars have been observed. Dektak 150 surface profileometer shows unevenness is more in locally fabricated solar cell than standard solar cell. Also aspect ratio is lower in the locally fabricated solar cells. Moreover, no oxygen and nitrogen gas has been used during metallization process as Gratings Inc.'s conveyer belt furnace does not provide any options to provide these gases.

These are the reasons for achieving low efficiency. Even though locally fabricated solar cell efficiency is low, problem identification will help and promote the scientists and researchers to identify and rectify the problems thus to increase efficiency of locally made solar cells in the near future.

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Chapter 6

SIMULATION OF SILICON SOLAR CELL

6.1 Introduction

Solar cell has come a lot further since 1839, when French experimental physicist Antoine-César Becquerel discovered photovoltaic effect [1-2]. Still, efficiency of the solar cell is limited, and commercially available silicon solar panel efficiency is about 13%. In all the cases of solar cell fabrication, the experimental procedure proves to be difficult for understanding, sometimes phenomena are not observable or measurements are impractical. Furthermore, little change in the solar cell fabrication process is too expensive. Because, change in any aspect of fabrication process is a difficult task, simulation has gained importance over the past few years and allowed the designers to change different parameters of the system thus enabling them to fabricate and observe behavior of the system [3]. Not only that, simulation has also provided the researchers to study and observe their theoretical investigations [4]. Last but not the least, simulation has vastly extended the range and depth of application with minimum cost, and better understanding how the things operate.

PC1D is a commercially available software most commonly used for solar cell modelling [5]. This software is currently used by many companies and universities like, University of New South Wales, Australia. Here PC1D version 5.9 has been used to simulate an energy efficient monocrystalline silicon solar cell. The simulation also gives insight about the range and impact of doping concentration, diffusion length, texturing and anti-reflection coating.

6.2 Simulation of Monocrystalline Solar Cell

Efficient and accurate modelling requires all the parameters of a solar cell to be involved. But for simplicity and to understand the impact of the parameters, some of the parameters like texturing and anti-reflection coating is not considered at first. Typically a solar cell thickness varies from 100 nm to 500 nm and normally the area is of 10×10 cm^2 or 12.5×12.5 cm^2 [6].

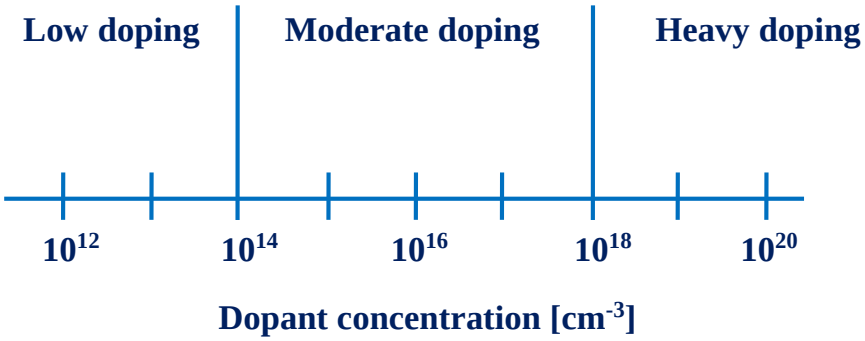


Figure 6.1 Range of Doping Concentration

So a *P*-type silicon wafer, with an area of 10 × 10 cm^2 and thickness of 300 µm has been selected for solar cell simulation. The doping concentration of monocrystalline silicon wafer varies from 1 × 12 cm^{-3} to 1 × 20 cm^{-3} as shown in Figure 6.1 [7]. High doping concentration in *P*-type wafer increases V_{oc} (open circuit voltage) but at the cost of damaging the crystal [8]. So, moderate doping is generally used in *P*-type silicon wafer. Thus, the doping concentration of *P*-type silicon wafer has been randomly adjusted to 5 × 16 cm^{-3} at first.

By using a four point probe instrument, it is seen that normally *P*-type wafer sheet resistivity varies form 0.01 Ω.cm to 10 Ω.cm. Because of variation in doping concentration, the sheet resistivity varies. It is seen that sheet resistivity decreases with the increase of doping concentration**.** For doping concentration 5 × 16 cm^{-3}, the *P*-type wafer sheet resistivity is 0.3441 Ω.cm [9]. So 0.3441 Ω.cm has been considered at first for simulation. The doping level of emitter (*N*-type) has been randomly adjusted to 1 × 19 cm^{-3} to form a *P*-*N* junction. For 1 × 19 cm^{-3} the emitter (*N*-type) sheet resistance is 26.11 Ω / □ (ohms/square). So 26.11 Ω / □ has been considered as sheet resistance of the emitter. Normally, the thickness of the emitter (*N*-type) varies form 1-2 µm. So in this simulation, the thickness of the emitter has been adjusted to 2 µm and uniform doping profile condition has been assumed. Diffusion length must be less than the thickness of *P*-type material. As thickness of *P*-type wafer is selected 300 µm so, at first, diffusion length has been randomly considered, 144.3 µm. To observe the impact of anti-reflecting coating (ARC), ARC is not applied at first. To emulate the sun, AM (Air Mass) -1.5 G condition has been selected. Also, to see the time progression, number of time steps has been selected to 100. After running the simulation, it is seen that, the efficiency of solar cell is 12.10 %.

In Figure 6.2, the blue line shows the *I*-*V* curve and the red line shows the *P*-*V* curve of 12.10% efficient solar cell. The current (*I*) versus voltage (*V*) curve of a solar cell shows all the possible combinations of its current and voltage outputs. Whereas (the red line), the power (*W*) versus voltage (*V*) curve shows all the possible combinations of its power and voltage outputs. The point in the *I*-*V* curve where, voltage and current is maximum is called maximum power point (MPP). In the *P*-*V* curve, MPP is the point where power has the highest value. In both *I*-*V* and *P*-*V* curve the maximum power point is represented as P_m. Also the maximum voltage and maximum current is designated as V_m and I_m. The value of short circuit current (I_{sc}), open circuit voltage (V_{oc}), I_m, V_m, P_m, efficiency and fill factor are shown in Table 6.1.

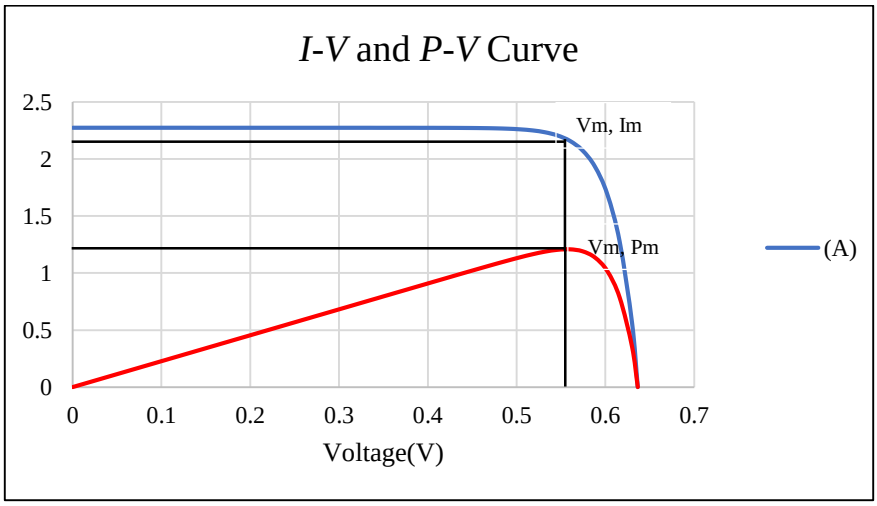


Figure 6.2 *I*-*V* and *P*-*V* Curve of 12.10% Efficient Solar Cell

TABLE 6.1: Data of 12.10 % Efficient Solar Cell

I_{sc}	V_{oc}	V_m	I_m	P_m	FF	Efficiency
2.28A	0.636V	0.56 V	2.16 A	1.21 W	0.835	12.10%

6.3 Impact of Doping Concentration

Doping concentration of *P*-type silicon wafer has been changed to find out the optimum doping concentration and its impact on the efficiency of the solar cell. At first, doping concentration of the emitter (*N*-type) has been kept fixed at 1×10^{19} cm^{-3}. Then the *P*-type silicon wafer doping concentration has been changed in the simulation. After completion of the simulation, the obtained data have been tabulated in Table 6.2 and the *I-V* curves for different doping concentration have been drawn and shown in Figure 6.3. In Figure 6.3, blue, red, green, violet, yellow, brown and black color represent the doping concentration of 1×10^{14} cm^{-3}, 1×10^{15} cm^{-3}, 1×10^{16} cm^{-3}, 1×10^{17} cm^{-3}, 1×10^{18} cm^{-3} and 5×10^{16} cm^{-3}, respectively.

From the simulated data, (Table 6.2 and Figure 6.3) it is seen that, increasing doping concentration does not always increases efficiency. Especially when, the *P*-type silicon wafer doping concentration is more than or closer to the doping concentration of *N*-type wafer, efficiency drastically decreases. Because of excessive doping, excess minority carrier lifetime is reduced, thus minority carrier diffusion length is also reduced [10]. Also, carrier mobility decreases with increasing total dopant concentration and thus reduces efficiency [11]. Low *P*-type doping concentration also shows poor result. Here, from the simulation optimum *P*-type doping concentration has been found $1x10^{17}$ cm^{-3}. As *P*-type doping concentration varies from 1×12 cm^{-3} to 1×20 cm^{-3} [7], the optimum *P*-type doping concentration falls within this range.

TABLE 6.2: Data of Solar Cell with Various *P*-type Doping Concentration

Material	Doping Concentration	Short Circuit Current (I_{sc})	Open Circuit Voltage (V_{oc})	Max Power (W)	Fill Factor (FF)	Efficiency
P-type	5×10^{16} cm^{-3}	2.275 A	0.6364 V	1.210 W	0.835745022	12.10%
P-type	1×10^{16} cm^{-3}	2.311 A	0.5953 V	1.138 W	0.827192207	11.38%
P-type	1×10^{14} cm^{-3}	2.439 A	0.4891 V	0.7964 W	0.667608394	7.964%
P-type	1×10^{15} cm^{-3}	2.343 A	0.5363 V	1.006 W	0.800604257	10.06%
P-type	1×10^{17} cm^{-3}	2.258 A	0.6526 V	1.236 W	0.838778836	12.36%
P-type	5×10^{17} cm^{-3}	2.184 A	0.6597 V	1.208 W	0.838431943	12.08%
P-type	1×10^{18} cm^{-3}	2.116 A	0.6543 V	1.160 W	0.837848325	11.60%
P-type	1×10^{19} cm^{-3}	1.592 A	0.5952 V	0.692 W	0.729981392	6.917%
P-type	1×10^{20} cm^{-3}	$-9.17e^{-5}$A	$2.20e^{-10}$V	-	-	-

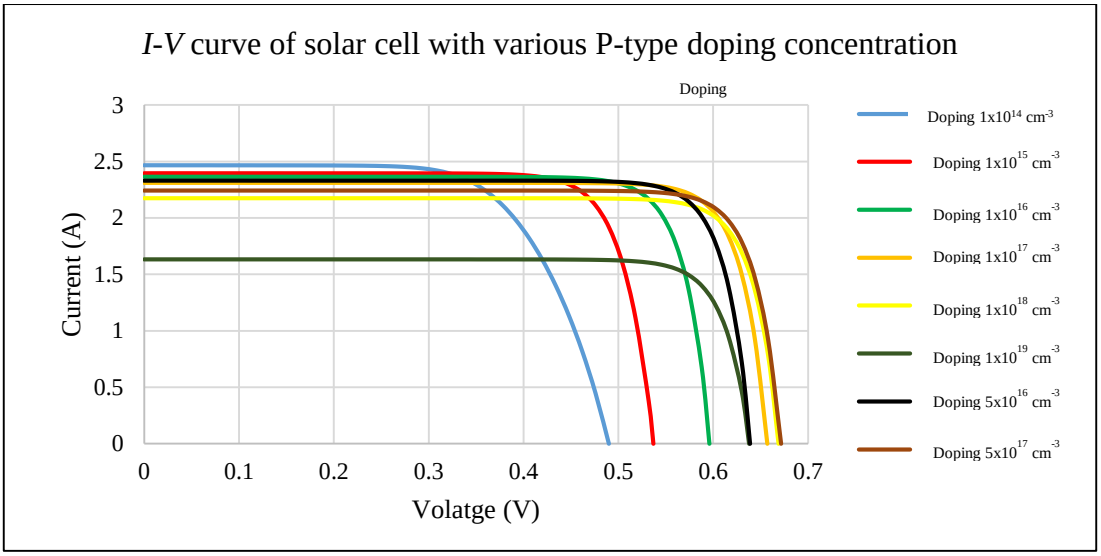


Figure 6.3 *I-V* Curve with Various *P*-type Doping Concentration (*N*-type Doping Concentration Fixed at 1×10^{19} cm^{-3})

Next, by keeping *P*-type doping concentration fixed at 5×10^{16} cm^{-3}, *N*-type doping concentration has been varied in PC1D simulation. After that both *P*-type and *N*-type doping concentration has been varied. The results have been tabulated in Table 6.3 and *I-V* curves are drawn as shown in Figure 6.4 and Figure 6.5 In Figure 6.4, black, red, green, brown, yellow and blue color represents *N*-type doping concentrations of 1×10^{19} cm^{-3}, 1×10^{20} cm^{-3}, 1×10^{18} cm^{-3}, 1×10^{17} cm^{-3}, 5×10^{18} cm^{-3} and 5×10^{17} cm^{-3}, respectively. In addition to that, in Figure 6.5 black, blue and red color respectively represents *N*-type doping concentration of 5×10^{17} cm^{-3}, 1×10^{18} cm^{-3} and 1×10^{19} cm^{-3} and *P*-type doping concentration of 5×10^{16} cm^{-3}, 1×10^{17} cm^{-3} and 1×10^{17} cm^{-3}, respectively. It is seen that, (Table 6.3, Figure 6.4 and Figure 6.5) optimum doping concentration of *P*-type wafer is 1×10^{17} cm^{-3} and *N*-type is 1×10^{18} cm^{-3}. At that doping concentration maximum efficiency is 12.94% with fill factor value 0.8395. It should be noted that for *N*-type doping concentration 1×10^{21} cm^{-3} and *P*-type doping concentration of 5×10^{16} cm^{-3} transient convergence failure occurs as shown in Table 5.3. The transient convergence failure indicates error in result [12] i.e. convergence for a transient simulation cannot provide an solution using PC1D simulation. This can be caused by a numerous factors, like time steps, non-linearity etc. Mainly because solar cell is a non-linear model for those parameters it is unable to provide result and for that transient convergence failure occurs.

TABLE 6.3: Data of Solar Cell with Various *N*-type and *P*-type Doping Concentration

Doping Concentration (*N*-type)	Doping Concentration (*P*-type)	Short Circuit Current (I_{sc})	Open Circuit Voltage (V_{oc})	Max Power (*W*)	Fill Factor (*FF*)	Efficiency
1×10^{19} cm^{-3}	5×10^{16} cm^{-3}	2.275 A	0.636 V	1.21 W	0.835745022	12.10%
1×10^{20} cm^{-3}	5×10^{16} cm^{-3}	1.433 A	0.608 V	0.72 W	0.830194943	7.232%
1×10^{21} cm^{-3}	5×10^{16} cm^{-3}	1.058 A	-	0.51 W	Transient Convergence Failure	
1×10^{18} cm^{-3}	5×10^{16} cm^{-3}	2.335 A	0.641 V	1.26 W	0.843573546	12.63%
1×10^{17} cm^{-3}	5×10^{16} cm^{-3}	2.356 A	0.641 V	1.26 W	0.836315286	12.63%

5×10^{18} cm^{-3}	5×10^{16} cm^{-3}	2.334 A	0.639 V	1.25 W	0.836128804	12.48%
5×10^{17} cm^{-3}	5×10^{16} cm^{-3}	2.356 A	0.641 V	1.26 W	0.836054427	12.63%
1×10^{18} cm^{-3}	1×10^{17} cm^{-3}	2.334 A	0.660 V	1.29 W	0.839510940	12.94%
1×10^{19} cm^{-3}	1×10^{17} cm^{-3}	2.258 A	0.653 V	1.24 W	0.838778836	12.36%

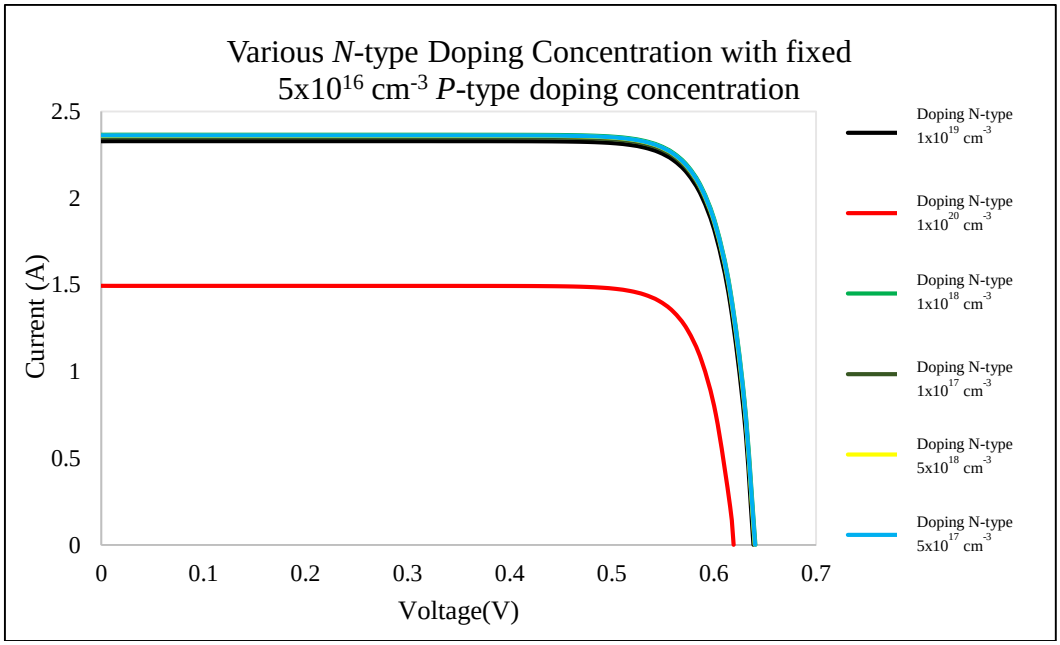


Figure 6.4 *I-V* Curve with Various *N*-type Doping Concentration (*P*-type Doping Concentration Fixed at 5×10^{16} cm^{-3})

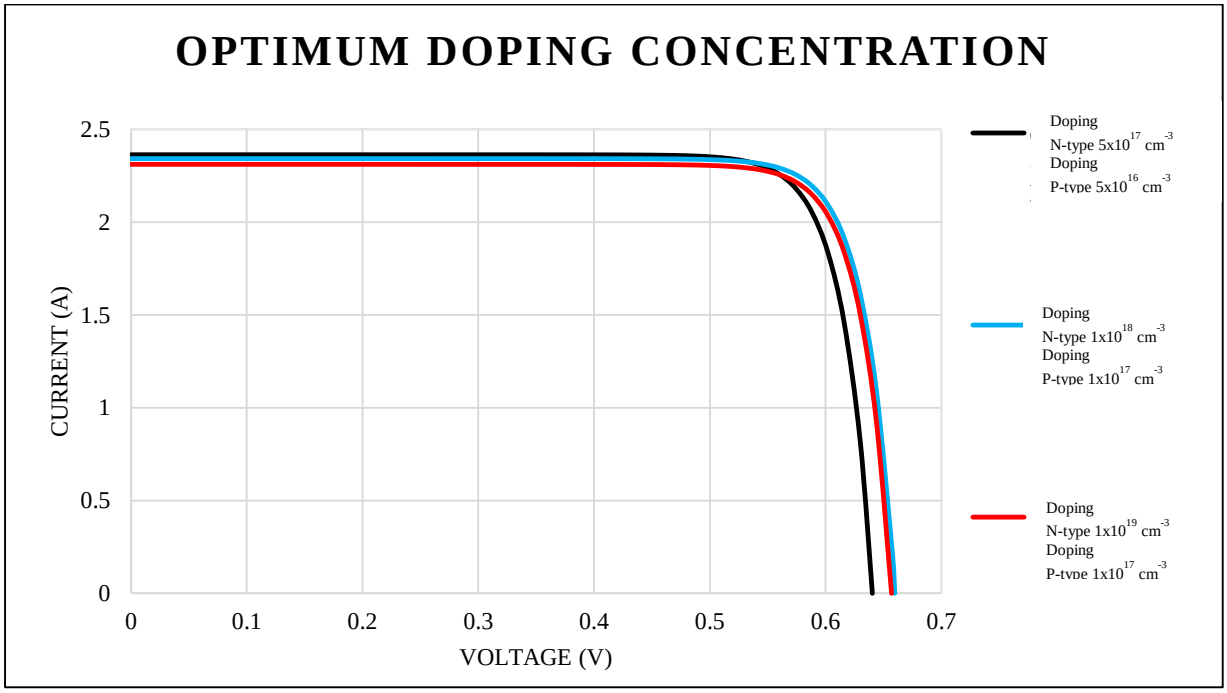


Figure 6.5 *I-V* Curve of Solar Cell with Optimum Doping Concentration

6.4 Impact of Diffusion Length

The key factor for improving the efficiency of solar cell is the minority-carrier lifetime [13]. The greater the minority carrier lifetime the larger is the efficiency of solar cells. The relationship between minority carrier life time and diffusion length is

$L = \sqrt{D\tau}$ [14].

Where L is the diffusion length in meters, D is the diffusivity in m^2/s and τ is the lifetime in seconds. Now, if diffusion length is increased, minority carrier life time is increased, thus efficiency of solar cell is increased. However, for monocrystalline silicon solar cell, typically the diffusion length is 100-300 µm [14]. Moreover, diffusion length must be less than the thickness of *P*-type material [15]. As *P*-type wafer thickness is 300 µm, maximum value of diffusion length is considered 200.3 µm. By observing some actual wafer specification it is seen that, the minimum minority carrier life time is 10 µs [16] (equivalent to diffusion length 130.5 µm). So diffusion length 130.5 µm is also used in the simulation. Lastly the lowest value of diffusion length 100 µm is used in the simulation. It is seen from Table 6.4 that, with optimum doping concentration and having 200.3 µm diffusion length the efficiency of the solar cell is 13.75%. It should be noted that, if diffusion length is increased more the efficiency will increase but for realistic approach the diffusion length is considered 200.3 µm.

TABLE 6.4: Data of Solar Cell with Different Diffusion (D_L) Length

Doping Concentration (*N*-type)	Doping Concentration (*P*-type)	Diffusion Length (Micrometer)	Minority Carrier Lifetime (µs)	Short Circuit Current (*Isc*)	Open Circuit Voltage (*Voc*)	Max Power (W)	Fill Factor (FF)	Efficiency
1×10^{18} cm^{-3}	1×10^{17} cm^{-3}	130.5	10	2.334 A	0.6604 V	1.294 W	0.839510940	12.94%
1×10^{18} cm^{-3}	1×10^{17} cm^{-3}	200.3	24.18	2.420 A	0.6744 V	1.375 W	0.84249973	13.75%
1×10^{18} cm^{-3}	1×10^{17} cm^{-3}	100	5.822	2.227 A	0.6522 V	1.245 W	0.857172718	12.45%

6.5 Texturization and Its Impact on Solar Cell

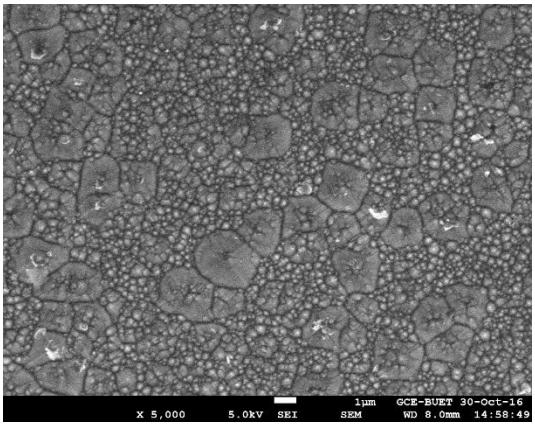
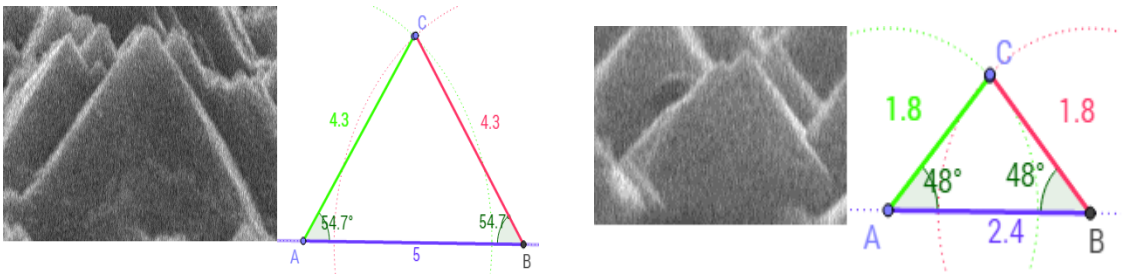


Figure 6.6 Textured Wafer

Texturization on solar cell is done to reduce reflection and enhance light absorption. Texturization normally creates uneven surface that is, pyramid like structures forms on the surface of *P*-type wafer as shown in Figure 6.6.

Texturization is normally done using wet chemicals. Here, a cleaned *P*-type wafer has been textured using 0.763 wt% KOH - 4 wt% IPA solution. Generally, pyramid height varies from 1-6 µm. By using a stylus surface profilometer the height of the peak of the pyramids has been measured. Result shows, pyramid height lies in the range of 1-3.5 µm. Also from the SEM image, pyramids angles have been measured using triangle maker software. Although pyramids angle being equilateral is theoretically possible but practically isosceles pyramid structures are formed. Measurement shows, isosceles pyramid having equal angles of maximum 54.74°. Pyramids having equal angles of 48° have also been found as shown in Figure 6.7.



(a) 54.74° (b) 48°

Figure 6.7 Isosceles Pyramid Angles

Now taking the value form the practically obtained data texturization has been done in the simulation. Both front surface and back surface texturization, only front surface texturization, only back surface texturization procedure has been done. Also, pyramids height and angles have been changed in the simulation. Simulation shows, for front and back surface textured wafer, having pyramids with height 2-3 µm and having an equal angle of 54.74° has the maximum efficiency of 14.02%. Similar results, have also been found for only front surface texturing, but as only one sided texturing is a difficult and costly procedure and after diffusion process it is difficult to identify the textured surface, both surface texturing is considered optimum. All the results from simulation have been tabulated in Table 6.5. It is found that texturization increases at least 1% to 2% efficiency of solar cell.

TABLE 6.5: Data of Textured Solar Cell

Doping Concentration 1×10^{18} cm^{-3} (*N*-type), 1×10^{17} cm^{-3} (*P*-type) D_L= 200.3	Short Circuit Current (*Isc*)	Open Circuit Voltage (*Voc*)	Max Power (*W*)	Fill Factor (*FF*)	Efficiency	Efficiency Increased
Not Textured	2.420 A	0.6744 V	1.375 W	0.84250	13.75%	$\frac{(1.402-1.375)}{1.375}*100$ = 1.96364%
Textured Front and Back Surface Textured Angle 54.74° Depth 3 µm	2.466 A	0.6748 V	1.402 W	0.84252	14.02%	
Textured	2.466 A	0.6748 V	1.402 W	0.84252	14.02%	$\frac{(1.402-1.375)}{1.375}*100$ = 1.96364%

Front and Back Surface Textured Angle 54.74° Depth 2 µm						
Textured Front and Back Surface Textured Angle 54.74° Depth 1 µm	2.466 A	0.6748 V	1.402 W	0.84252	14.02%	$\frac{(1.402-1.375)}{1.375}$*100 = 1.96364%
Textured Front and Back Surface Textured Angle 54.74° Depth 5 µm	2.465 A	0.6747 V	1.401 W	0.84238	14.01%	$\frac{(1.401-1.375)}{1.375}$*100 = 1.8909%
Textured Front and Back Surface Textured Angle 48° Depth 3 µm	2.454 A	0.6747 V	1.395 W	0.84254	13.95%	$\frac{(1.395-1.375)}{1.375}$*100 = 1.454545%
Textured Front Surface Textured Angle 54.74° Depth 2 µm	2.466 A	0.6748 V	1.402 W	0.84252	14.02%	$\frac{(1.402-1.375)}{1.375}$*100 = 1.96364%
Textured Back Surface Textured Angle 54.74° Depth 2 µm	2.420 A	0.6744 V	1.374 W	0.84189	13.74%	$\frac{(1.395-1.375)}{1.375}$*100 = 1.454545%

6.6 Impact of Anti-Reflection Coating

Anti-Reflection Coating (ARC) shows the most significant change in efficiency in this simulation. To design the ARC layer, the following equations [15] have been used to determine the thickness and refractive index of ARC layer.

Refractive index of ARC is $\eta_{AR} = \sqrt{\eta_{air} * \eta_{si}(\lambda_0)}$

And the thickness of ARC is d = $\frac{\lambda_0}{4 * \eta_{AR}}$

Using both the equations, thickness and refractive index of ARC layer has been calculated and shown in Table 6.6

TABLE 6.6: Thickness and Refractive Index of ARC Layer

Wavelength (nm)	Refractive Index of Silicon [17]	Refractive Index of ARC	Thickness (nm)
250	1.694	1.301538	48.02013

300	5.055	2.248333	33.35805
400	5.587	2.363684	42.30685
500	4.293	2.071956	60.32948
550	4.077	2.019158	68.09768
600	3.939	1.984691	75.5785
650	3.844	1.960612	82.88228
700	3.774	1.942679	90.08181
750	3.723	1.929508	97.17505
800	3.681	1.918593	104.243
900	3.62	1.90263	118.2574
1000	3.57	1.889444	132.314

Now varying the refractive index and thickness of ARC in the simulation efficiency of solar cell have been calculated and tabulated as shown in Table 6.7. It is seen that, if the thickness of ARC layer is 74 nm then the maximum efficiency of 20.35% can be achieved. If thickness of ARC layer is higher (e.g. 100 nm) than or lower than (e.g. 68 nm) 74 nm then the efficiency decreases. That is, for 74 nm thickness solar spectrum is absorbed more effectively.

TABLE 6.7: Data of Anti-Reflection Layer Coated Solar Cell

Doping Concentration 1×10^{18} cm^{-3} (*N*-type), 1×10^{17} cm^{-3} (*P*-type) D_L= 200.3 (Textured)	Short Circuit Current (I_{sc})	Open Circuit Voltage (V_{oc})	Max Power (W)	Fill Factor (FF)	Efficiency
No ARC	2.466 A	0.675 V	1.402 W	0.8426441910261158	14.02 %
Thickness 750nm, RI=2	3.059 A	0.680 V	1.756 W	0.844057940251561	17.56 %
Thickness 118nm, RI=1.9	3.232 A	0.682 V	1.860 W	0.8443295914098452	18.60 %
Thickness 60nm, RI=2.071	3.461 A	0.684 V	1.997 W	0.8439386672539161	19.97 %
Thickness 68nm, RI=2.019	3.511 A	0.684 V	2.027 W	0.8439239825584603	20.27 %

Thickness 74nm, RI=2.019	3.524 A	0.684 V	2.035 W	0.8438824864402391	20.35 %
Thickness 100 nm, RI=2.019	3.347 A	0.683 V	1.929 W	0.844202458217777	19.29 %

6.7 Result and Discussion

TABLE 6.8: Comparison Table

Parameters of Solar Cell	Published Literature/ Experimental Value	Simulated Optimum Value	Remark
P-type Doping concentration Range	1×12 cm^{-3} to 1×20 cm^{-3} [7]	1×17 cm^{-3}	Optimum value is within the range
N-type Doping concentration Range	1×12 cm^{-3} to 1×20 cm^{-3} [7]	1×18 cm^{-3}	Optimum value is within the range
Diffusion length	100-300 µm [14]	200.3 µm	Optimum value is within the range
Textured Wafer Pyramid Height	1-6 µm [18] 1-3.5 µm (Experimental)	2-3 µm	Optimum value is within the range
Textured Wafer Pyramid Angle	60° (Theoretical) 54.78° (Experimental)	54.78°	Optimum value is within the range
ARC layer thickness	30-135 nm [19]	74 nm	Optimum value is within the range

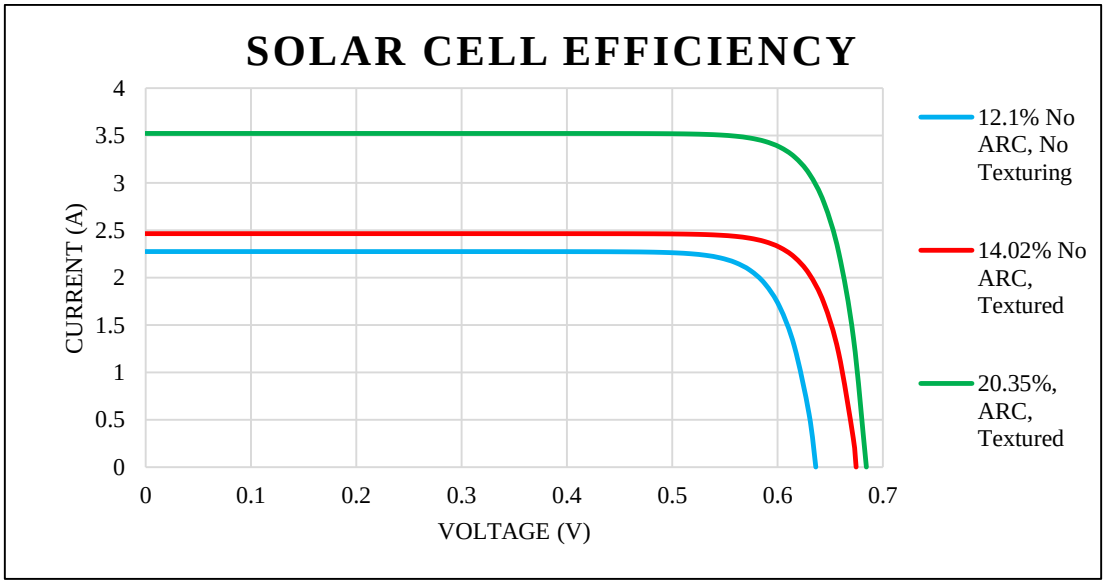


Figure 6.8 20.35% Efficient Solar Cell *I-V* Curve

The result obtained by simulation shows that, with *P*-type doping concentration 1×10^{17} cm^{-3}, *N*-type doping concentration 1×10^{18} cm^{-3}, diffusion length 200.3 µm, both side textured wafer (pyramid height 2-3 µm and equal angle of 54.74°) and with anti-reflection Coating thickness of 74 nm and refractive index 2.019, maximum cell efficiency of 20.357% can be achieved.

These optimum parameters are compared with published literature and found that the values are feasible and within the same range. In Figure 6.8, the blue curve represents *I-V* curve of solar cell with no ARC and texturing. The red curve represents *I-V* curve of solar cell with no ARC but textured surface. Finally the green curve represents *I-V* of solar cell with ARC and texturing. The blue curve also represents the initial simulation having 12.10% efficient solar cell. Then this solar cell has been optimized by proper application of ARC and texturization process and thus making a 20.35% efficient solar cell (green curve).

6.8 Summary

Simulation of monocrystalline silicon solar cell has been done by PC1D software. All the optimum parameters of solar cell have been determined using the simulation and are compared with published literature and found that the values are feasible. By the assist of experimentally obtained values, the texturization process has been thoroughly investigated in PC1D simulation. It can be said that applying texturing effect on solar cell at least 1-2% increase in efficiency is to be expected in real world solar cell fabrication scenario. This could be claimed that, the key accomplishment is by thoroughly investing different process, especially texturization, and optimizing different parameters in PC1D simulation, more than 20% efficient solar cell has been obtained. Simulation facilitates us by making better decisions thus it is one of the cost saving strategies for engineering [20]. Thus, promoting simulation of solar cell before actual fabrication may minimize lot of cost and in-depth reason what to expect by changing the parameters.

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Chapter 7

SIMULATION OF ANTI-REFLECTION COATING

7.1 Introduction

One of the important issues of modern photovoltaic science is the optical losses in solar cell. In general, the optical losses account for about 7% efficiency loss in crystalline silicon solar cells [1]. So, the reduction of optical loss can have a huge positive impact on the conversion efficiency of silicon solar cells [2]. To reduce the optical loss, anti-reflection coating (ARC) plays a pivotal role. It reduces reflection and increases the conversion efficiency of solar cells [3]. Anti-reflection coating reduces reflection by using the concept of phase changes of light and the dependency of the reflectivity on refractive index [4]. Although in the fabrication of solar cell, many researchers used different ARCs, still searching for a suitable ARC is going on which can be used to improve the efficiency of solar cell [5-6].

In the experimental study of ARC, Hocine *et al*. used TiO_2 on crystalline silicon solar cell and found an increased efficiency of 14.26%, whereas without TiO_2 the efficiency is limited to 11.24% [7]. Similarly Swatowska *et al*. found an efficiency of 9.84% for a crystalline silicon solar cell without any ARC, and efficiencies of 14% and 14.25% are obtained using TiO_2 and Si_3N_4, respectively [8]. In another study, Gee *et al*. fabricated 15.55% and 16.03% efficient crystalline silicon solar cell using TiO_2 and ZnO, respectively [9]. It thus, turns out that ZnO would be an appropriate choice among those different ARCs. However, in all cases the wafer size, fabrication process and the condition has been different. For instance, Hocine *et al*. used a 5×5 cm^2 wafer and Swatowska *et al*. considered 10×10 cm^2 wafer. Thus comparing different works is really a challenge and result cannot be always conclusive. Moreover, designing ARC is a difficult task because of having so many options in parameters and materials. Even a little change in any aspect of ARC fabrication in industry is challenging and costly. Therefore researchers are now giving importance in doing simulation before going to actual fabrication. This is because through simulation, parameters can be defined and changed, similar environment can be considered in all cases, and selection of materials can be done quite easily. Moreover, theoretical investigations can be observed and studied in depth [10].

In the simulation study of ARC, Abdullah *et al*. [6] used Silvaco ATLAS to simulate silicon solar cell and obtained 4.72% efficient solar cell using 5 nm SiO_2 coating. Lennie *et al*. also carried out simulation using the similar tool Silvaco ATLAS and showed that 4.56% efficient silicon solar cell can be simulated by using double layer SiO_2/Si_3N_4 anti-reflection coating [11]. In references [12-15] there are reports on simulation work using PC1D. Although same software has been used in all their works, however different ARC and materials have been used by them. For instance, Moradi *et al*. found 10.78%, 11.7% and 11.89% efficiency using TiO_2, ZnO and Si_3N_4 single layer ARC upon silicon solar cell respectively [13]. Also the efficiencies of 13.37% and 13.59% are shown using ZnO/TiO_2 and SiO_2/TiO_2 double layer ARC, respectively. Thosar *et al*. simulated GaAs solar cell and showed that optimum short circuit current can be found using ZnO and MnO ARC with 65 nm and 80 nm thicknesses,

respectively. [14]. Daniel N. Wright *et al.* reported 6.7% efficient solar cell with Si_3N_4 and SiO_2 ARC upon crystalline silicon wafers [12]. Yahia *et al.* performed simulation using Matlab to see the effects of ARC on silicon substrate [16]. From these researches, it is clear that Matlab, PC1D, Silvaco ATLAS are used to simulate ARC of solar cell [11-12, 16]. However, Matlab software does not provide rigorous options of solar cell. On the other hand PC1D is the most commercially available software used by many companies and universities [17]. Also, depending upon availability PC1D version 5.9 has been used to simulate solar cell with different types of ARC layer.

The vast majority of ARC simulation studies indicate, generally two or three single layer of ARC upon silicon solar cell gives 3-13% efficiency [6,12-16]. However, no report is found showing the suitable wavelength for designing ARC and utilizing the concept of surface passivation upon ARC. Thus, to overcome all these issues and to perform a systematic study the main goal of this work is to simulate different types of ARC and find out the suitable ARC for crystalline silicon solar cell. In this research, the impacts without ARC and with six types of ARC such as Titanium dioxide (TiO_2), Zinc oxide (ZnO), Zinc sulfide (ZnS), Silicon dioxide (SiO_2), Silicon nitride (Si_3N_4) and Silicon carbide (SiC) have been investigated separately for crystalline silicon solar cell. Furthermore, simulation ranging from 250 nm to 1200 nm wavelength has been conducted to find out the most suitable wavelength required for designing ARC in solar cell. Surface passivation upon ARC has been applied and its impact has been investigated. The ARC simulation also gives insight about its effects on efficiency of solar cell. Moreover, the reflectivity for the wavelength range of 250 nm to 1250 nm of all the ARCs and external quantum efficiency has also been discussed in this chapter.

7.2 Simulation

7.2.1 Simulation without ARC

To simulate the solar cell without ARC (Figure 7.1(a)), a *P*-type silicon wafer with an area of 10×10 cm^2 and thickness of 300 µm has been chosen. The doping concentration of *P*-type has been selected to 1×10^{17} cm^{-3}. Then the subsequent *N*-type silicon layer thickness and doping concentration has been adjusted to 2 µm and 1×10^{18} cm^{-3}, respectively [18]. In both *P*-type and *N*-type layer a uniform doping profile has been assumed. Typically, the diffusion length of mono-crystalline silicon solar cell is 100-300 µm [19].

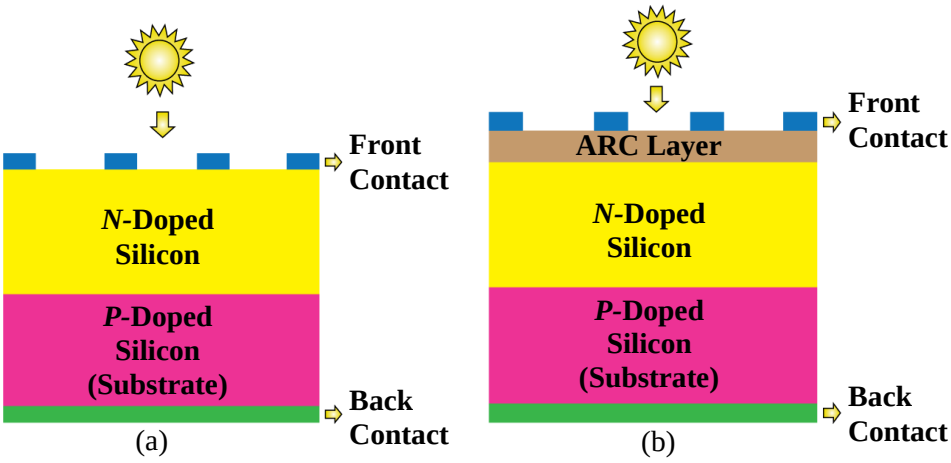

Figure 7.1 Simplified Solar Cell Structure. (a) Without ARC (b) With ARC

The diffusion length has to be less than the *P*-type wafer thickness which is 300 µm. The minimum minority carrier life time limits the diffusion length less than 130 µm [20]. Thus for realistic approach the diffusion length of 200 µm is considered here. To enhance the absorption, experimentally obtained textured wafer data has been considered and inputted in this simulation. Both sides texturing option is enabled and pyramid height of 1 µm with equal angles of 54.74 degrees is considered for initial simulation. This is because in reference [18] the pyramid heights of textured wafer are in the range of 1-3.5 µm, and obtained the following etching solution of 0.763 wt% KOH - 4 wt% IPA. Finally, to simulate the sun, AM (Air Mass) 1.5 G and 100 number of time steps have been selected.

7.2.2 Simulation with different ARC

To introduce ARC layer, the front surface "optically coated" option has been selected in the simulation. Then the refractive index and thickness have been varied according to different ARCs. A simplified solar cell schematic with ARC is shown in Figure 7.1 (b). Now, in order to design and understand the behavior of the ARC layer, the following equations [21-24] are necessary.

$$\hat{n}(\lambda) = n(\lambda) + i\kappa(\lambda) \quad \ldots\ldots(1)$$

Where $\hat{n}(\lambda)$ is the complex refractive index. In complex refractive index there is real part called real refractive index $n(\lambda)$, and an imaginary part called extinction coefficient $\kappa(\lambda)$ and both are function of wavelength. The absorption coefficient $\alpha(\lambda)$ is related to the extinction coefficient k by the following relation

$$\alpha(\lambda) = \frac{4\pi}{\lambda}\kappa(\lambda) \ldots.(2)$$

From equation 2 it is clear that the photons (or radiation) that are absorbed depend on the wavelength, thickness and nature of the medium [24].

Now the refractive index of ARC is $\eta_{ARC} = \sqrt{\eta_{air} * \eta_{arc}(\lambda_0)}$ …. (3)
and the thickness of ARC is $d = \frac{\lambda_0}{4*\eta_{ARC}}$…. (4)

Here, η_{air} is the refractive index of air and η_{arc} is the refractive index of an anti-reflection coating for a specific wavelength (λ_0). Closer inspection of equation 3 shows that refractive index of ARC depends on refractive index of air as well as wavelength dependent refractive index of a particular anti-reflection coating. Nevertheless, the value of right hand side of equation 3 is not inputted in equation 3 or in the simulation. From the reference [25-30] experimentally obtained η_{ARC} values for different ARC ranging from 250-1200 nm has been directly inputted in the equation 4 and then in the simulation. Inputting wavelength (λ_0) and corresponding η_{ARC} value determines the associated optimum thickness values for each ARC. All the wavelength, thickness, refractive index, V_{oc}, I_{sc} and efficiency are tabulated in Table 7.1. Then with the optimum thickness and its corresponding η_{ARC} values, performances of different ARC layers have been studied through reflectance. It is well known that, high surface recombination rate reduces short circuit current and thus the efficiency of solar cells. The surface recombination of photo-excited electron-hole pair takes place because of the dangling bonds at the top of surface. By reducing the number of dangling bonds surface recombination

can be reduced. Generally, a technique called thermal oxidation is used to reduce the surface recombination. In thermal oxidation technique a "passivating" layer is grown thermally. The surface passivating layer is fabricated with silicon oxide (SiO_2) which is used to passivate the surface. By applying only O_2 gas SiO_2 layer can be grown upon Si_3N_4 layer [31]. As Si_3N_4 ARC shows the highest efficiency (discussed in section 7.3.1), in this work, surface passivated layer that is a simulation of SiO_2 layer upon Si_3N_4 ARC layer has been done.

In the simulation, to see the external quantum efficiency and reflectivity of each ARC layer, excitation option has been modified from "one sun" to "SCAN-QE" (scan quantum efficiency). Furthermore, for better analysis, number of time steps has been increased to 200 and the monochromatic wavelength spectrum range has been selected from 250 nm to 1250 nm. Then the simulation data of external quantum efficiency and reflectivity has been obtained and analyzed for every single ARC.

7.3 Results and Discussion

7.3.1 Effects of ARC

By analyzing the data of different ARCs (in Table 1) it is seen that changing wavelength along with its thickness also changes the V_{oc}, I_{sc} and the efficiency of the solar cell. As absorption coefficient, refractive index, excitation coefficient, are wavelength dependent and cannot be changed easily so only thickness of the film can be optimized to get optimum absorption to maximum V_{oc}, I_{sc} and efficiency. In the case of SiC the table reveals that optimum thickness of SiC ARC is 36.159 nm. For that thickness maximum 16.06% efficiency has been achieved. Maximum V_{oc} and I_{sc} value of 0.6779 V and 2.807 A is achieved at the best efficiency. The optimum thickness and efficiency with TiO_2, ZnO, ZnS, SiO_2 and Si_3N_4 ARC for solar cell are 62.396, 78.411, 63.479, 101.351 and 74.257 nm and 19.73%, 20.34%, 19.83%, 18.99% and 20.35%, respectively. The reason for such efficiency increase is the reduction of light reflection [32]. As the thickness increases then V_{oc}, I_{sc} and efficiency also increases up to the point where reflection is lowest (Figure 7.2). Then V_{oc}, I_{sc} and efficiency of solar cell decreases as reflection increases. So optimization of thickness is required to get the lowest reflectance and to obtain the best V_{oc}, I_{sc} and efficiency. Surprisingly except SiC ARC, for all other ARCs the highest efficiency is achieved at a wavelength of 600 nm. Thus reflectance curve ranging from 250-1250 nm of all ARC designed for 600 nm wavelength and associated thickness is shown in Figure 7.2. It is seen that at a wavelength of 600 nm, for SiC, TiO_2, ZnO, ZnS, SiO_2 and Si_3N_4 ARC the reflectances are 24.31%, 3.59%, 0.136%, 2.98%, 8.14% and 0.032%, respectively. Overall the lowest reflectance curve (Green) is for Si_3N_4 ARC closely followed by the Red reflectance curve of ZnO ARC. The Black curve shows the general representation of a solar cell reflectance curve without any ARC.

It can be seen from the Black curve that there are two peaks and afterwards the curve decreases and then it becomes somewhat constant. But for all the reflectance curves with ARC, after two peaks the curves decrease rapidly up to a point then again increases. It is in good agreement of the results shown in Table 1, as the similar behavior is observed in the case of efficiency. The summary of Table 7.1 is that for 74.257 nm thick Si_3N_4 ARC for solar cell shows the best result, 20.35% efficiency is found.

TABLE 7.1: Data of Different ARC

	SiC-ARC					TiO_2-ARC					ZnO-ARC				
λ	Refractive Index [25]	Thickness (nm)	*Isc* (A)	*Voc* (V)	*η*	Refractive Index [26]	Thickness (nm)	*Isc* (A)	*Voc* (V)	*η*	Refractive Index [27]	Thickness (nm)	*Isc* (A)	*Voc* (V)	*η*
250	3.25	19.231	2.655	0.6765	15.14%	2.46	25.407	2.789	0.6777	15.95%	2.388	26.173	2.797	0.6778	16.00%
300	3.528	21.259	2.649	0.6765	15.10%	3.326	22.55	2.712	0.677	15.49%	2.404	31.198	2.937	0.6791	16.84%
400	3.519	28.417	2.75	0.6774	15.72%	2.68	37.213	3.313	0.6808	18.00%	2.114	47.304	3.269	0.682	18.82%
500	3.457	36.159	2.807	0.6779	16.06%	2.48	50.403	3.358	0.6828	19.36%	1.968	63.516	3.467	0.6838	20.01%
600	3.406	44.04	2.802	0.6778	16.03%	2.404	62.396	3.42	0.6834	19.73%	1.913	78.411	3.523	0.6843	20.34%
700	3.358	52.114	2.773	0.6776	15.86%	2.364	74.027	3.377	0.683	19.47%	1.883	92.937	3.473	0.6839	20.04%
800	3.315	60.332	2.736	0.6772	15.63%	2.341	85.434	3.247	0.6821	18.85%	1.864	107.296	3.359	0.6829	19.36%
900	3.285	68.493	2.702	0.6769	15.44%	2.325	96.774	3.156	0.681	18.14%	1.851	121.556	3.226	0.6817	18.56%
1000	3.247	76.994	2.686	0.6768	15.34%	2.313	108.085	3.06	0.6802	17.57%	1.841	135.8	3.109	0.6806	17.86%
1100	3.228	85.192	2.708	0.677	15.47%	2.305	119.306	2.997	0.6796	17.19%	1.833	150.027	3.023	0.6798	17.35%
1200	3.2	93.75	2.719	0.6771	15.54%	2.298	130.548	2.953	0.6792	16.93%	1.826	164.294	2.963	0.6793	16.99%
	ZnS-ARC					SiO_2-ARC					Si_3N_4-ARC				
λ	Refractive Index [28]	Thickness (nm)	*Isc* (A)	*Voc* (V)	*η*	Refractive Index [29]	Thickness (nm)	*Isc* (A)	*Voc* (V)	*η*	Refractive Index [30]	Thickness (nm)	*Isc* (A)	*Voc* (V)	*η*
250	2.6	24.038	2.771	0.6776	15.85%	1.52	41.12	2.757	0.6774	15.76%	2.289	27.304	2.805	0.6779	16.05%
300	2.57	29.183	2.909	0.6788	16.67%	1.51	49.67	2.87	0.6785	16.44%	2.167	34.61	2.962	0.6793	16.99%
400	2.56	39.063	3.176	0.6812	18.26%	1.5	66.67	3.097	0.6805	17.79%	2.07	48.31	3.271	0.6821	18.83%
500	2.421	51.632	3.382	0.6831	19.50%	1.482	84.35	3.242	0.6818	18.66%	2.03	61.576	3.468	0.6838	20.01%
600	2.363	63.479	3.437	0.6836	19.83%	1.48	101.351	3.297	0.6823	18.99%	2.02	74.257	3.525	0.6843	20.35%
700	2.332	75.043	3.39	0.6831	19.55%	1.474	118.72	3.263	0.682	18.79%	2.003	87.369	3.475	0.6839	20.05%
800	2.324	86.059	3.28	0.6821	18.89%	1.473	135.78	3.18	0.6813	18.29%	1.996	100.2	3.361	0.6829	19.37%
900	2.31	97.403	3.161	0.6811	18.17%	1.472	152.85	3.078	0.6803	17.68%	1.991	113	3.227	0.6817	18.57%
1000	2.301	107.648	3.071	0.6803	17.63%	1.471	169.95	2.984	0.6795	17.11%	1.987	125.82	3.113	0.6806	17.88%
1100	2.296	119.774	2.999	0.6796	17.20%	1.47	187.07	2.911	0.6788	16.68%	1.985	138.54	3.031	0.6799	17.40%
1200	2.29	131.004	2.954	0.6792	16.94%	1.469	204.22	2.86	0.6784	16.37%	1.983	151.28	2.974	0.6794	17.06%

It is fascinating that without any ARC the efficiency of solar cell is 14.02%. So, after applying ARC significant increase in efficiency is observed. Now to find out the explanation of decrease of reflectance up to a certain point and then an increase in the reflectance curve in Figure 7.2, more simulation on Si_3N_4 ARC has been conducted as Si_3N_4 ARC indicates the best solar cell efficiency. Simulation results are shown in Table 7.2.

From Table 7.2 it is seen that if Si_3N_4 ARC is designed for 500 nm wavelength and with 61.576 nm thickness then the reflectance is lowest at 500 nm. At 500 nm Si_3N_4 ARCs reflectance is 0.045% whereas at 600 and 700 nm the reflectance is 3.677% and 8.957% respectively. Similarly if Si_3N_4 ARC is designed for 600 nm wavelengths and with 74.257 nm thickness then reflectance at 500, 600 and 700 nm are 5.537%, 0.0317% and 2.644%, respectively. Thus exciting observation from the Table 7.2 is that, the particular wavelength and associated thickness for which the ARC is designed has the lowest reflectance. So in all the ARC reflectance curves in Figure 7.2, the reflectance decreases after the two peaks up to 600 nm wavelength and associated thickness for which the ARC has been designed. Observing all the reflectance curves in Figure 7.2 it can be concluded that when the reflection of light from the surface is reduced the efficiency of solar cell is increased.

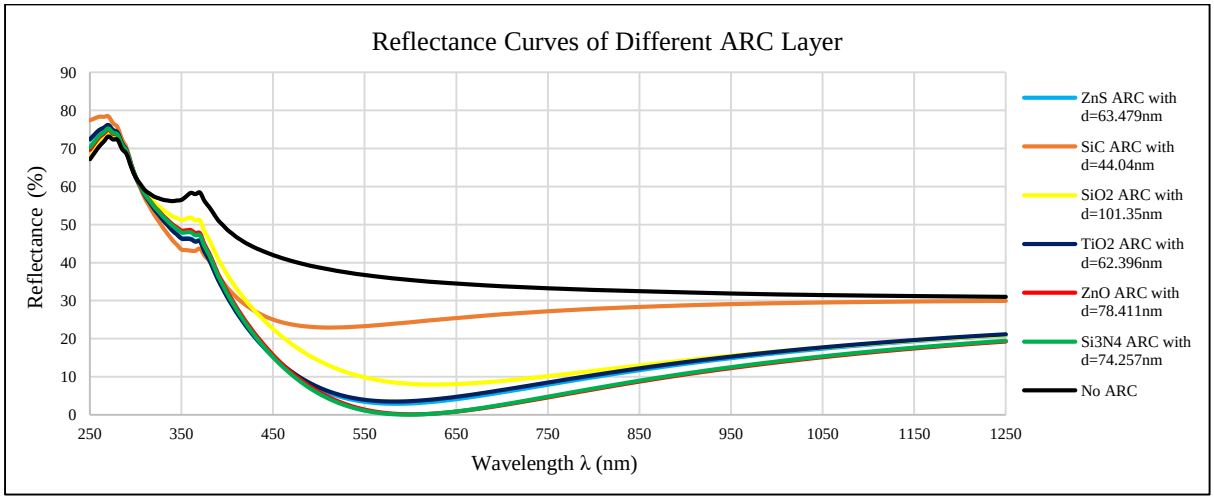

Figure 7.2 Reflectance Curves of Different ARC Layer (Designed for 600 nm Wavelength with Associated Thickness)

TABLE 7.2: Data of Si_3N_4 ARC

ARC (Si_3N_4)	Reflectance (%) at 500 nm Wavelength	Reflectance (%) at 600 nm Wavelength	Reflectance (%) at 700 nm Wavelength	Efficiency
λ=500 nm, d = 61.576 nm	0.045	3.677	8.957	20.01%
λ= 600 nm, d = 74.257 nm	5.537	0.0317	2.644	20.35%
λ =700 nm, d = 87.369 nm	17.716	3.462	0.094	20.05%

7.3.2 Effects of surface passivation

As stated earlier solar cell with Si_3N_4 ARC has the best efficiency of 20.35%, with surface passivation (SiO_2 layer) applied only upon this layer. Table 7.1 indicates the optimum thickness of SiO_2 and Si_3N_4 layer are 101.351 nm and 74.257 nm, respectively thus these two thicknesses have been used in the simulation for surface passivation first and after completion of simulation the data are tabulated in Table 7.3. It indicates that maximum of 20.42% efficiency can be achieved by applying 101.351 nm thick SiO_2 layer upon 74.257 nm thick Si_3N_4 layer. However, through optimization the layer thickness can be reduced as seen from Table 3 that, optimum efficiency of 20.67% is being achieved with 57 nm thick SiO_2 layer upon 58 nm thick Si_3N_4 ARC. This is because the SiO_2 surface passivated layer upon Si_3N_4 ARC behaves like double layer ARC and for that refractive index, thickness and reflectivity of the ARC layer follows a complex equation. Details are given in the reference [33]. It is also evident that optimum surface passivation reduces both SiO_2 and Si_3N_4 layer thickness thus in actual fabrication process overall fabrication cost may be reduced. The reflectivity curve in Figure 7.3 also confirms the complex behavior of surface passivated layer. Unlike the Si_3N_4 ARC (green curve) there is an increase in reflectance around 600 nm regions for surface passivated blue curve. Whereas the surface passivated red reflectance curve overall has lower reflectance in the 250-1250 nm wavelength region than other reflectance curves. The fact is that the efficiency is increased due to the reduced of reflection of light which is because of surface passivation process.

TABLE 7.3: Associate Parameters of Solar Cell with Surface Passivated ARCs

Surface Passivation Conditions	Short Circuit Current (I_{sc})	Open Circuit Voltage (V_{oc})	Max Power (W)	Fill Factor (FF)	Efficiency
101.351 nm SiO_2 / 74.257 nm Si_3N_4 ARC	3.535 A	0.6844 V	2.042	0.8440	20.42%
57 nm SiO_2 / 58 nm Si_3N_4 ARC	3.576 A	0.6848 V	2.067	0.8441	20.67%

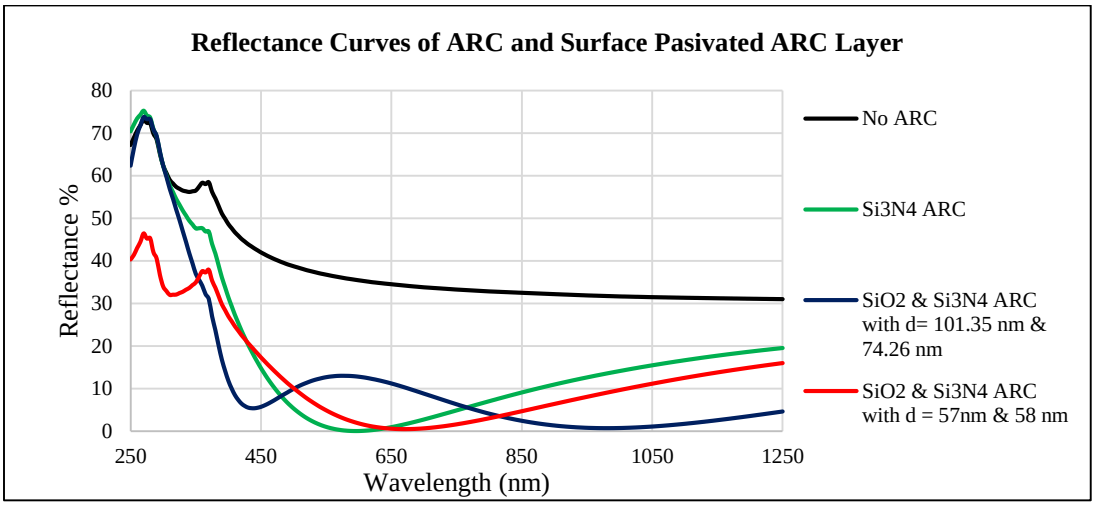

Figure 7.3 Reflectance Curves of ARC and Surface Passivated ARC Layer

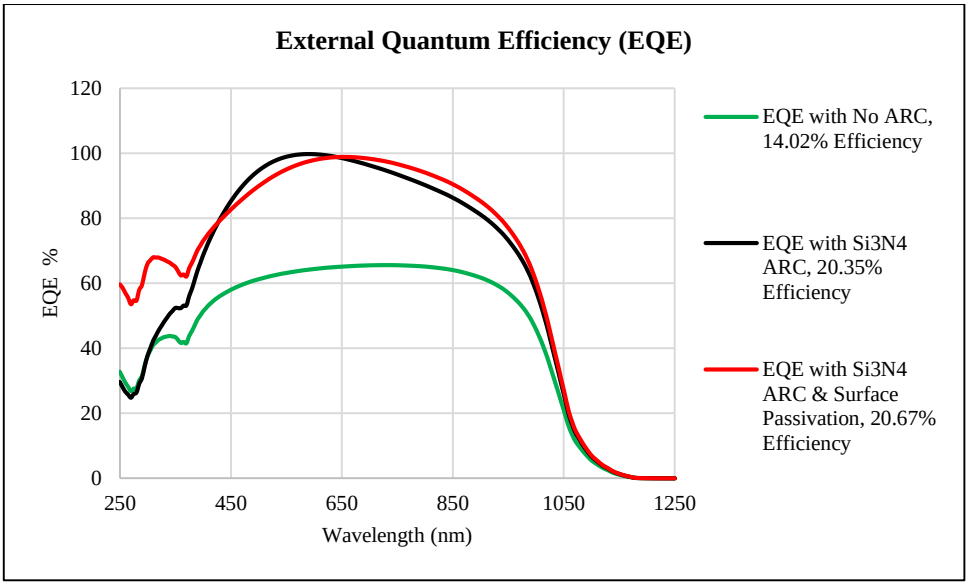

Figure 7.4 External Quantum Efficiency Curves

The values of external quantum efficiency (EQE) is shown in Figure 7.4. From Figure 7.4, it can be concluded that after utilization of ARC, EQE has increased significantly. This increase is due to the reduction of reflection for applying ARC. Although from 425 nm to 640 nm the EQE of Si_3N_4 ARC (Black) curve is slightly greater than EQE of Si_3N_4 ARC (Red) curve, from 640 nm and overall the EQE is showing the best result for the surface passivated curve (Red). It is adequate to say, surface passivation increases the overall EQE of solar cell by reducing the number of dangling bonds thus reducing the recombination effects [34-35].

7.4 Summary

The effect of different single layer ARC has been investigated using PC1D simulation software. Simulation shows that the wavelength range 500 nm – 700 nm would be suitable for designing an ARC. Among TiO_2, ZnO, ZnS, SiO_2, Si_3N_4 and SiC of 20.35% efficiency is found of Si_3N_4 ARC solar cell. Then, ZnO ARC is indicating the second best performance with an efficiency of 20.34%. However, without any ARC the efficiency of solar cell is 14.02%. So, after applying ARC significant increase in efficiency is observed. The reason for such efficiency increase is due to the reduction of reflection. So applying anti reflection coating would be a good choice to enhance the efficiency. Also SiO_2 surface passivation treatment on Si_3N_4 ARC layer has been performed and 20.67% efficient solar cell is achieved. Increase in EQE and decrease in reflectance also confirms that surface passivated layer upon ARC increases the efficiency of solar cell.

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Chapter 8

BAND GAP MEASUREMENT OF SILICON WAFER

8.1 Introduction

One of the most important properties of a semiconductor that distinguishes it from metals and insulators is band gap. Band gap is defined as the energy difference (in eV) between the lowest energy level of upper band (conduction band) and the highest level of energy of the lower band (valence band) in insulators and semiconductors. [1] Furthermore, band gap measurement has a significant role in semiconductor, nanomaterial and solar cell fabrication industries [2].

As band gap measuring equipment's are very costly sometimes resource management is necessary. For this purpose, the main goal of this research work has been to utilize an equipment rather than its primary purpose. Although, the primary purpose of spectral response measurement system is to measure the spectral response of a material, this system has been used to measure the band gap of *P*-type monocrystalline silicon wafer. Details about the band gap measurement process of *P*-type monocrystalline silicon wafer has been discussed in this chapter. The measurement shows that, the band gap of polished *P*-type monocrystalline silicon wafer is 1.127907 eV. Furthermore, the band gap of silicon has been theoretically calculated which is 1.127362 eV. There are various techniques like UV-VIS spectroscopy, Tauc's plot and equation, reflection, and absorption coefficient or spectra, four point probe etc. are used to determine the band gap of semiconductor. But here only partial concepts of Tauc's method has been used. Additionally, spectral response of polished *P*-type monocrystalline silicon wafer has been investigated. Then, this result has been theoretically verified by calculating the photon energy with Planck–Einstein relation and relating the photon energy with band gap of silicon (1.12eV).

8.2 Spectral Response Measurement System Description

The spectral response measurement system, as shown in Figure 8.1, is composed of a SR510 lock in amplifier, SR540 optical chopper, monochromator (400nm-1200nm), optical detector and Lab View software. This system emits and directs lights upon a material and form the reflected lights it determines the spectral response of a material [3]. Here, light emits from a tungsten-halogen lamp which is then focused onto the entrance slit of the monochromator using a condenser lens. Furthermore, a stepper motor is attached to the monochromator which rotates and varies the monochromator output wavelength between 400 nm to 1200 nm. Also a SR540 optical chopper is placed at the exit slit of the monochromator to provide reference signal to the SR510 lock-in amplifier to ensure all the stray light is rejected by the system and enhance system sensitivity from nV to mV range. The output from the monochromator is directed to the material (silicon wafer) with a simple rotating mirror. After that, the reflected light falls upon a large convex lens close to the surface of the material thus collecting the reflected and scattered light which is then focused onto an optical detector.

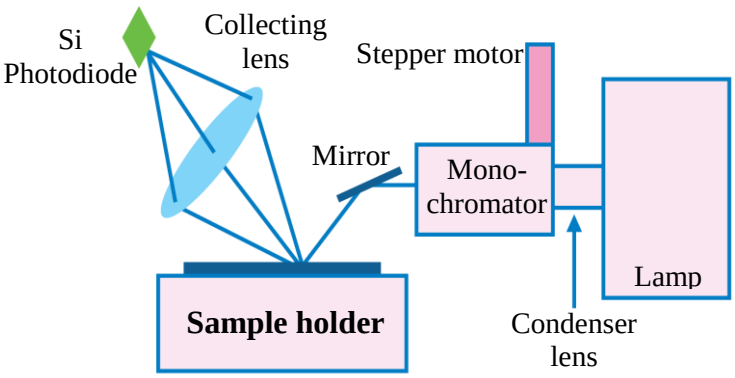

Figure 8.1 Schematic Diagram of Spectral Response Measurement System

The optical detector (which converts optical signal to electrical signal) is connected to SR510 lock-in amplifier for measurement through the Lab View interface. Here, Lab View interface is used for system control, data acquisition and view the spectral response of the material. The primary purpose of the spectral response measurement system is to plot the spectral response of a material and then from the plotted graph relative reflectivity (in respect to mirror/sample) can be obtained.

8.3 Spectral Response of Polished P - type Monocrystalline Silicon Wafer

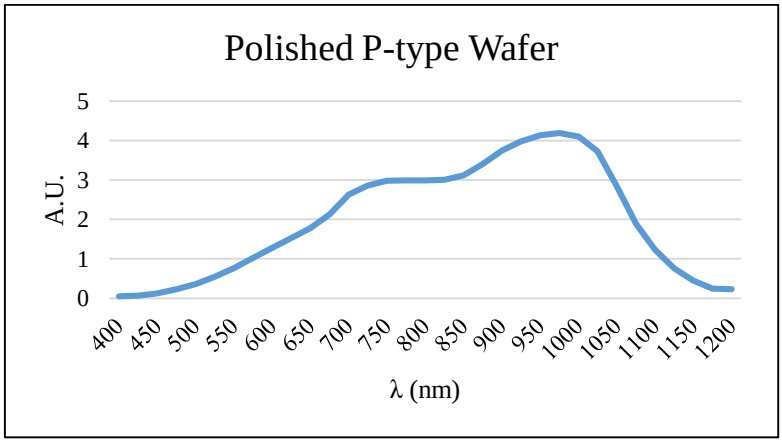

Figure 8.2 Spectral Response of Polished P - type Monocrystalline Silicon Wafer

Figure 8.2 shows the spectral response of polished *P*-type monocrystalline silicon wafer. To interpret the spectral response it is important to understand the relationship between photon energy and band gap. It is seen that, if the (photon energy) $h\upsilon > E_g$ (Band gap) then absorption will happen [4]. The amount of absorption will depend upon refractive index, absorption coefficient, thickness, surface roughness etc. of the semiconductor material. Moreover, if $h\upsilon = E_g$ then electron hole pair is created and light is efficiently absorbed. Whereas, if $h\upsilon < E_g$ then light interact weakly and pass through the semiconductor as if it is a transparent material. So to see, these relationship, the Planck-Einstein equation has been used to determine the photon energy of different wavelength by the following equation.

$E = h\upsilon$ …. (1)

Where h is the Planck constant, E is the photon energy and υ is the associated wave frequency.

Or, $E = \frac{hc}{\lambda}$ [5] $= \frac{(4.135667516 \times 10^{-15} eVs)(299792458\ ms^{-1})}{\lambda}$

This equation can be reduces to

E (eV) $= \frac{1239.84193}{\lambda\ (nm)}$ …. (2)

From equation (2) photon energy of different wavelength along with its corresponding frequency and color are calculated and given in Table 8.1.

TABLE 8.1: Photon Energy of Different Wavelength

Color	Wavelength	Frequency	Photon energy
violet	380–450 nm	668–789 THz	2.75–3.26 eV
blue	450–495 nm	606–668 THz	2.50–2.75 eV
green	495–570 nm	526–606 THz	2.17–2.50 eV
yellow	570–590 nm	508–526 THz	2.10–2.17 eV
orange	590–620 nm	484–508 THz	2.00–2.10 eV
red	620–750 nm	400–484 THz	1.65–2.00 eV
Infrared	700 -1050 nm	430 THz-300 GHz	1.24 mili eV-1.7eV

Now, the band gap of silicon is 1.12 eV [6-7]. So, photon energy more than 1.12 eV will get highly absorbed. Therefore, when 400-550 nm (violet to green, photon energy 2.75-2.50 eV) wavelength falls on the *P*-type wafer these wavelength is highly absorbed. As the wavelength increases (from red to infrared wavelength (550-1050nm)) the photon energy becomes lower and as photon energy become close to silicon band gap 1.12 eV, absorption decreases and reflection increases. At 975 nm, peak is observed, where reflection is highest. After infrared region photon energy is lower than band gap of silicon (1.12eV) so transmittance happen, so roll off of spectral response is seen.

8.4 Literature Review and Theoretical Calculation of Band Gap of Silicon

Although most of the books and journals specified band gap of silicon as 1.12 eV, literature review of band gap of silicon suggests that the band gap of silicon varies from 1.11 eV to 1.13 eV. This is due to the fact that, as temperature varies, the intrinsic carrier concentration (n_i), effective density of states of the conduction band (N_c) and effective density of states of the valance band (N_v) also varies. The theoretical and experimental parameters values are considered different in different books and journals and that's why the band gap of silicon varies from 1.11 eV to 1.13eV. However, it is suffice to say that the band gap of silicon will always lie between 1.11 eV to 1.13eV.

Theoretical Band Gap of Silicon Calculation:

At first thermal voltage V_T has been calculated using the following equation:

$$V_T = \frac{KT}{q} = \frac{1.380 \times 10^{-23} \times 300}{1.602 \times 10^{-19}} = 0.2584 \text{ V}$$

Where *K* is the Boltzmann constant, *T* is the temperature in Kelvin and *q* is the electron charge in coulomb.

Now, the conduction band energy at intrinsic level is determined by the following equation

$$E_c = V_T \times ln\left(\frac{N_c}{n_i}\right)$$

Where, N_c is the conduction band state concentration (at intrinsic) = 2.86 x 10^{19} (cm^{-3}) [8]

And n_i is the intrinsic carrier concentration of silicon = 1 x 10^{10} cm^{-3} [9-10]

Therefore, conduction band voltage E_c = 0.02584 $ln \frac{2.86 \times 10^{19}}{1 \times 10^{10}}$ = 0.562642 eV

Now, the valance band energy at intrinsic level is determined by the following equation

$$E_v = - V_T \times ln\left(\frac{N_v}{n_i}\right)$$

Where, N_v is the valance band state concentration (at intrinsic) = 3.10 x 10^{19} cm^{-3} [8]

Therefore, valance band voltage E_v = - 0.02584 $ln \frac{3.10 \times 10^{19}}{1 \times 10^{10}}$ = - 0.56472 eV

Now, the band gap (E_g) of silicon is

$E_g = E_c - E_v$

E_g= 1.127362 eV

8.5 Band Gap Measurement

Various techniques like UV-VIS spectroscopy [11], Tauc's plot and equation, reflection, and absorption coefficient or spectra, four point probe etc. are used to determine the band gap of semiconductor. However, here only partial concept of Tauc's, downhill negative slope intersection point with horizontal axis is used. Major difference between Tauc's band gap measurement process [12-13] and this work is that, Tauc's band gap measurement process uses the photon energy (eV) vs. absorption coefficient plot of the material whereas here, arbitrary unit (A.U.) and wavelength (λ) of the material has been used to determine the band gap of semiconductor.

8.5.1 Band Gap Measurement of *P*-type Monocrystalline Silicon Wafer Using Spectral Response Measurement System

To determine the band gap of *P*-type monocrystalline polished silicon wafer, the spectral response of *P*-type monocrystalline silicon wafer has been drawn from the measured data (Table 8.2). After that, drawing of a negative slope along the downhill part of the spectral response of *P*-type monocrystalline polished silicon wafer must be done, as shown in Figure

8.3. Now, to draw the negative slop along the downhill spectral response, downhill part spectral data are selected from Table 8.2 (Highlighted by yellow color).

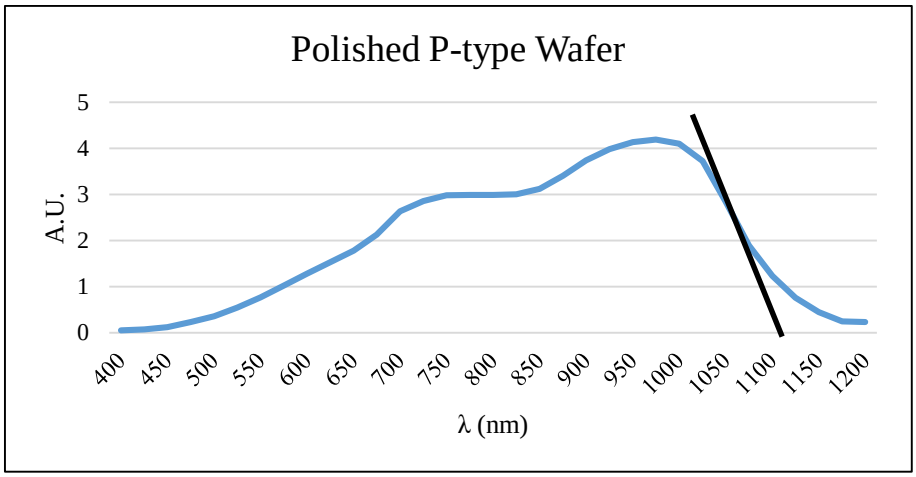

Figure 8.3 Negative Slope (Drawn along Downhill Part of Spectral Response of Polished *P* - type Monocrystalline Silicon Wafer)

TABLE 8.2: Spectral Response Data of *P*-Type Monocrystalline Polished Silicon Wafer

Wavelength (nm)	Arbitrary unit (A.U.)	Wavelength (nm)	Arbitrary unit (A.U.)	Wavelength (nm)	Arbitrary unit (A.U.)	Wavelength (nm)	Arbitrary unit (A.U.)
400	0.050524	625	1.5301	850	3.117777	1075	1.890594
425	0.069366	650	1.7814	875	3.402314	1100	1.231275
450	0.122354	675	2.1298	900	3.740745	1125	0.758917
475	0.232614	700	2.6319	925	3.978037	1150	0.445094
500	0.360011	725	2.8547	950	4.135528	1175	0.246814
525	0.547155	750	2.9837	975	4.188643	1200	0.229275
550	0.764653	775	2.9900	1000	4.098329	1075	1.890594
575	1.02386	800	2.9901	1025	3.724194	1100	1.231275
600	1.279529	825	3.0029	1050	2.840405	1125	0.758917

From the highlighted color at least 3 wavelengths along with A.U (Arbitrary Unit) are needed to from a straight line. Here it can easily be done using Microsoft Excel software. Just selecting and then removing the unnecessary points (wavelengths) will easily form a straight line, which is actually the negative slope (shown in Figure 8.4). The negative slope formation wavelengths and associated A.U. are tabulated in Table 8.3.

TABLE 8.3: Negative Slope Formation from the Three Wavelengths

Wavelength (nm)	Arbitrary unit (A.U.)
1025	3.724194
1050	2.840405
1075	1.890594

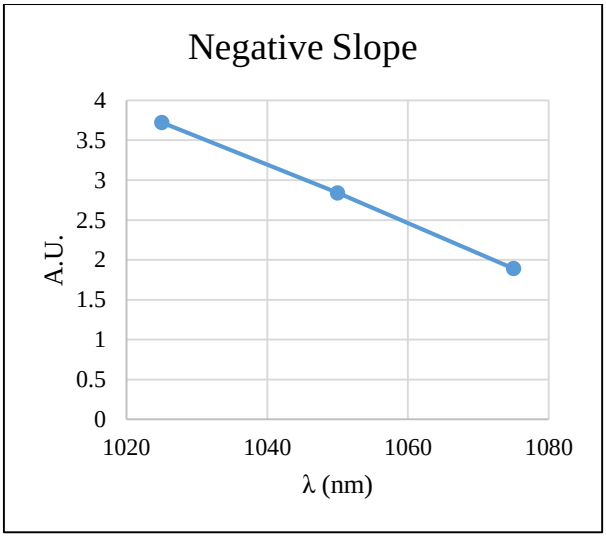

Figure 8.4 The Three Wavelengths and Associated AU Which form the Negative Slope

Now, extension of the negative slope will intersect the horizontal axis. The intersection wavelength along horizontal axis is necessary for determining the band gap. To find out the intersection point of horizontal axis, three point P_1 (1050, 2.840405); P_2 (1075, 1.890594); P_3 (λ, 0) have been considered. These three points are in the same line. It is only possible if and only if the slope for both the lines are same. As λ is the intersection point of horizontal axis all these points will be in the same line and slope will be the same.

So, m (slope) = $\frac{y_1-y_2}{x_1-x_2} = \frac{y_1-y_3}{x_1-x_3}$

$\frac{3.84045-1.890594}{1050-1075} = \frac{3.840405-0}{1050-x_3}$

$\frac{1.949811}{-25} = \frac{3.840405}{1050-x_3}$

$1.949811(1050-x_3) = -96.010125$

$2047.30155-1.949811x_3 = -96.010125$

$-1.949811x_3 = -2143.311675$

Therefore, x_3 or λ = 1099.240734 nm

Now putting the wavelength value in equation 2 we get,

Band Gap = $\frac{1239.84193}{1099.240734}$ =1.127907eV; which is the band gap of *P*-type monocrystalline silicon wafer.

8.6 Result

The theoretical calculation shows the band gap of silicon is 1.127362 eV and experimental result shows the band gap is 1.127907eV. So the error is $\frac{1.127907-1.127362}{1.127362} \times 100 = 0.04834\%$, which can be considered negligible.

8.7 Summary

Although the relative reflectivity is normally measured by spectral response measurement system, it is seen that band gap of polished *P*-type monocrystalline silicon wafer can also be measured by this system. Experimental measurement shows band gap of silicon is 1.127907eV. Whereas, theoretical calculated value is 1.127362 eV. The error is only 0.04834%, which can be considered as negligible. With this spectral response measurement system the absorption coefficient cannot be determined, so direct and indirect band gap semiconductor identification is not possible. But, it can be concluded that spectral response measurement equipment can be used as a band gap measurement equipment if the semiconductor material spectral response lies between 400 nm to 1200 nm. The main purpose of this work has been to use an equipment rather than its primary purpose. As spectral response measurement system can measure the band gap of silicon the primary purpose of this work has been fulfilled. Furthermore, from spectral response of polished *P*-type mono-crystalline silicon wafer absorption, reflection and transmission has been observed and the result has been theoretically verified using Planck–Einstein relation.

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Chapter 9

TEXTURIZATION OF AS-CUT *P*-TYPE MONOCRYSTALLINE SILICON WAFER

9.1 Introduction

A lot of attention is now being given to the solar cell industry to increase the efficiency of the solar cell. It is seen that the conversion efficiency of silicon solar cells mainly depends upon optical losses and electrical losses [1]. Moreover, the reduction of optical losses in monocrystalline silicon solar cells can be achieved by random texturization process which is one of the important issues of modern photovoltaic science. The random texturization process causes uneven pattern on the surface and thus causing reduction of the reflection [2]. At present, both wet chemical processing and dry etching are used for texturization process [3-5]. However, wet chemical based texturization process is most widely used in industrial application because the texturization process needs to be time and cost efficient [6-8].

Therefore, depending upon high volume of production, low manufacturing cost, light trapping and most importantly to reduce reflectivity of monocrystalline silicon wafer surface, various wet chemical texturization process have been developed over the last few years [9]. Among all texturization recipes KOH (Potassium Hydroxide)-IPA (Isopropyl Alcohol) is the most commonly used recipe in the solar cell industry. However, the concentration, temperature and process time is not fixed. It is seen that the concentration of KOH varies between 1 to 40% and the temperature between 70°C to 90°C [10-12]. The process time variation remains below one hour [13]. As KOH is harmful if inhaled and handling of KOH requires more precautions, recently the researches have been concentrating on investigating new texturing methods and alternative solutions. In 1999, Nishimoto and Namba [14] presented Na_2CO_3 (sodium carbonate) solution as an alternative to the KOH/IPA solution for the first time. Nishimoto's work has been later modified by Sparber *et al*. [6] who used 11.8 wt% Na_2CO_3 and 1.5 wt% $NaHCO_3$ (sodium bicarbonate) solution for 40 minutes at 90°C. Later notably Amada *et al*. [15] used 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$ solution and found optimum reflection for 30 min of texturization. In 2015, JunJun *et al*. used 20 wt% Na_2CO_3-4 wt% $NaHCO_3$ solution for texturization process. Another unorthodox texturization recipe is the use of Tetramethylammonium hydroxide (TMAH) solution. However, a suitable recipe involving TMAH has not yet been established in the solar cell industry [16-17].

Since there are lots of texturization recipes, the main goal of this research work is to find out the optimum recipe for texturization based on timing, concentration and temperature. In this work, texturing experiment has been carried out on a 200 µm thick, as-cut monocrystalline silicon wafer using 0.76 wt% KOH-4 wt% IPA, 1.9 wt% KOH-4.7 wt% IPA, 11.8 wt% Na_2CO_3-1.5 wt% $NaHCO_3$, 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$ and 1 wt% TMAH-4 wt% IPA solution with different time durations. Apart from texturization process, saw damage removal process has also been investigated. Saw damage removal process is completed prior to

texturization process with different wet chemical solutions. Here, for saw damage removal process, 10% NaOH, 20 wt% KOH-13.33 wt% IPA and HNA (Hydrofluoric acid, Nitric acid and Acetic acid) solution with different time durations has been used**.** Although the recipe uses the same wet chemicals as that used by Nishimoto *et al*., JunJun *et al*., Amada *et al*. Rosa *et al*., etc. but the target wafer, saw damage removal procedures, and processing time are different in this work. Nishimoto and Namba used polished *P*-type wafer and cleaned the wafer in HF solution (less than 10 wt%), Amada *et al*. used as-cut *P*-type monocrystalline wafer and cleaned the wafer in 30 wt% NaOH solution at 83°C, JunJun *et al*. used 20 wt% Na_2CO_3 and 4 wt% $NaHCO_3$ solution for 30 min at 85°C, Rosa *et al*. used a 4 inch polished c-Si wafer and of etched for 40 min in 2%TMAH solution at 80°C. In prior arts it is observed that KOH concentrations varies from 1 wt% to 5 wt%, IPA concentrations from 3% to 7% and the temperatures from 70°C to 90°C. Here in this work, less than 1 wt % KOH concentration has been considered. Impact of greater than 1 wt% KOH concentration has also been observed. In addition, 1 wt% TMAH with 4 wt% IPA concentrated solution texturization process has also been exploited which is a different recipe than Rosa *et al.* [16] and Papet *et al.* [17]. Different saw damage removal procedures are used and all the saw damaged removed and textured wafers reflectivity has been measured from 250 nm to 840 nm using UV-VIS NIR spectrophotometer. Furthermore, surface morphology of saw damage, saw damage removed surface and textured wafer has been observed using optical microscope and FE-SEM. Sheet resistance has also been measured. Finally, angles and the height of the peak of the pyramids of textured wafer have been measured and the results are presented and discussed in this chapter.

9.2 Experimental Details

9.2.1 Spectrophotometer Calibration and Experimental Setup

This paper discusses more elaborately the reflectance of a material. So proper acquisition of reflectance data using spectrophotometer is crucial for understanding the actual behavior of the material. Fundamentally, there are two techniques that is used to measure reflectance of a material. They are relative reflectance and absolute reflectance. The absolute reflectivity of all the samples have been measured by a Hitachi UH4150 (ultraviolet-visible-near infrared) UV-VIS-NIR spectrophotometer. The system measures absolute reflectance by using the V-N method. The spectrophotometer also uses a 60 mm integrating sphere to measure the total reflectance. For all measurements, the spectral range of UV-VIS-NIR spectrophotometer has been fixed in between 250 to 840 nm. Selected scan speed value is 600 nm/min and PMT (Photomultiplier tube) voltage has been adjusted to 600 V. After selection of wavelength, PMT and scan speed the system baseline measurement has been performed without placing any sample. The baseline shows 100% reflectance if the system works perfectly. Then, a sample can be placed in the sample holder for reflectance measurement. However, with the selection of wavelength, PMT and scan speed the polished and saw damaged removed samples data can only be obtained. If a material (i.e. textured wafer) has low reflectance, the reflectance data cannot be detected due to the noise. So, for measuring low reflectance samples attenuation option must be enabled. Here, for textured samples, attenuation has been set to 0.1 to reduce noise. No significant change has been observed when the value of attenuation is set to 0.01. Furthermore, the UV-VIS-NIR system does not measure weighted average reflectivity. Here, all the works have been dealt with measurement of absolute reflectivity only.

9.2.2 Base Material

Monocrystalline silicon is used as the base material for silicon chips and the silicon chips are widely used in electronic and photovoltaic industry. Depending upon the surface condition of the monocrystalline silicon, the wafer is categorized as polished and as-cut wafer. Both polished and as-cut monocrystalline wafers are commercially available in the market. Absolute reflectance for polished wafer measured using spectrophotometer, shows that the reflectance value is in the range of 37.1-19.7% (Figure 9.1) within 250-800 nm wavelength region. Whereas for as-cut wafer the reflectance is very low and lies in between 1.049-0.75% (Figure 9.2) within 250-800 nm wavelength region. So, there is a significant difference in reflectance between polished and as-cut wafer, although they are both monocrystalline silicon wafer. The reason for such difference is the surface of the polished wafer which is very smooth and shiny and behaves like a mirror and hence produces high reflectance. Conversely, the surface of as-cut wafer is very rough and the material is gray in color, which obviously gives returns a low reflectance value.

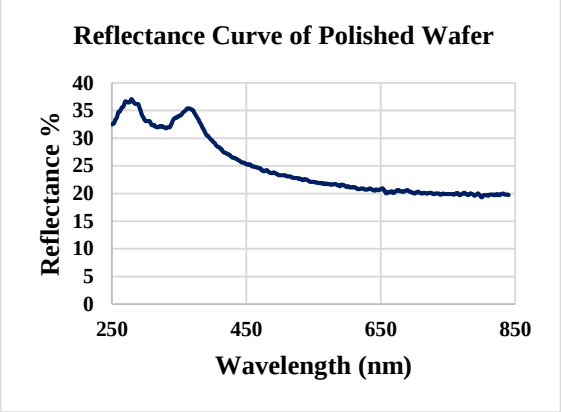


Figure 9.1 Reflectance Curve of Polished Monocrystalline Silicon Wafer

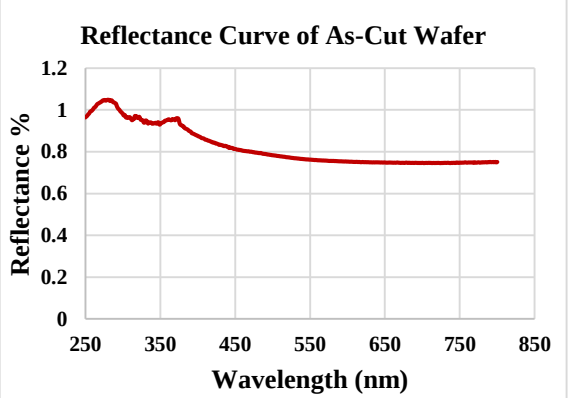


Figure 9.2 Reflectance Curve of As-Cut Monocrystalline Silicon Wafer

Polished monocrystalline silicon wafer does not need saw damage removal process. Thus experiments have been carried out to see the effect of saw damage removal process and the impact of texturization on as-cut wafer. All the substrates used in all the experiments are commercially available Renesola Company *P*-type, as-cut, (100) oriented, monocrystalline silicon wafer with a thickness of 180 ± 20 µm. The as-cut wafer is called 'as-cut' because the silicon wafers surface are damaged due to the action of the saw. To ensure whether the substrate is damaged or not, the surface morphology have been inspected by using FE-SEM. It would be challenging to fabricate a well aligned and uniform solar cell if the near surface saw damage layer is not removed properly. Moreover, the probability of surface recombination increases due to decreasing trend of penetration of *N*-type dopant [18]. For this reason, the saw damaged surface should be removed and the removal process in this work has been carried out by using wet chemical solutions which is known as saw damage removal process.

9.2.3 Saw damage removal Process

Saw damage removal process of as-cut monocrystalline silicon wafer has been conducted by RCA-1 and Piranha solution separately. By solely using RCA-1 or Piranha solution, the saw damage removal process cannot be completed or it may take very long time. In order to confirm this impact on saw damaged surface the substrate has been immerged in RCA-1 (a 5:1:1

mixture of DI-W, 27% NH_4OH, and H_2O_2 at 70°± 5°C) and Piranha solution (a 3:1 mixture of H_2SO_4 and H_2O_2 at 100°C) for 15 min separately.

To remove the saw damaged surface, normally high concentration (> 5%) of aqueous alkali solution of NaOH or KOH is used [19-20]. In this work, the saw damage removal process has been carried out in two steps. In the first step, the *P*-type as-cut monocrystalline silicon wafer has been submerged in 10% NaOH solution at 70-80°C with different time durations of 10, 30 and 40 min. In the second step, 20 wt% KOH-13.33 wt% IPA solution at 70-75°C has been used for a duration of 20, 25, 30, 35 and 40 min. Acidic solutions are other options and also widely used to remove the saw damage of the substrate [21]. Thus, in the last trial of saw damage removal process, the substrate has been immerged for 5 min in a HNA solution, which is a mixture of 250 ml HF, 500 ml HNO_3 and 800 ml CH_3COOH. After completion of the saw damage removal process, the surface morphology of all the substrates has been inspected by Micros Square (DS-600) optical microscope. Keithlink IV four point probe measurement system has been used to measure the sheet resistance of saw damaged and without saw damaged wafers.

9.2.4 Texturization

As stated earlier, texturization process causes uneven pattern on the surface and resulting in formation of pyramidal microstructures on the silicon surface. These microstructures are able to redirect the reflected light with appropriate angle which then impinge again on the silicon surface, thus reduces reflection. To form pyramidal microstructures on silicon surface, different texturization processes have been examined. Primarily for all texturization process, saw damage removal process has been performed by 10% NaOH solution at 70-80°C for 10 min. Texturing is then carried out using KOH-IPA solution with two different concentrations (0.76 wt% KOH-4 wt% IPA and 1.9 wt% KOH-4.7 wt% IPA). The texturization process temperature is kept between 70°C to 80°C and the time variation for both process are 10, 20, 25, 30, 35 and 40 min. The other route of texturization is followed using 11.8 wt% Na_2CO_3-1.5 wt% $NaHCO_3$ and 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$ solution with varied time durations of 10, 20, 30, 40 and 50 min. In both processes the solution temperature is 70-80°C. Lastly, 1 wt % TMAH with 4 wt % IPA solutions has been also used for 20 and 40 min at 80°C.

Here, it is worth noted that the impact of texturization without saw damage removal process has been also observed. After cleaning the substrates with RCA-1 and Piranha solution separately, texturization process (without saw damage removal) with 0.76 wt% KOH - 4 wt% IPA solution with various time duration at 70 to 80°C has been carried out.

During all the texturization process, the substrates are flipped after passing of halftime. The absolute reflectivity of all textured substrates has been measured by a Hitachi UH4150 UV-VIS-NIR spectrophotometer.

The surface morphology of the textured surfaces has been inspected by Genesys logic USB digital microscope. The topography of the textured surface has been observed by JEOL JSM-7600F field emission scanning electron microscope (FE-SEM). The FE-SEMs field emission gun has been operated at 5 kV. Furthermore, the sheet resistance of the textured substrates has been measured by using KiethLink IV four point probe system. The angles and height of the pyramids of the textured wafer has been also measured.

9.3 Results and discussion

9.3.1 Saw damage and saw damage removed substrate

Monocrystalline silicon ingots are sliced by internal diameter (ID) or wire saw to obtain as-cut wafer. After cutting the wafer with saw, the wafer surface gets damage due to sawing. FE-SEM confirms that the commercially available ReneSola as-cut, *P*-type monocrystalline silicon wafer surface is damaged due to the action of the saw as shown in Figure 9.3. A similar SEM image of saw damaged surface has been obtained by Park *et al.* [21]. It is seen that the damaged surface is rough and gray in color. After cleaning the saw damaged substrate with RCA-1 and Piranha solution, the surface remains unchanged and it is verified by FE-SEM inspection. RCA-1 and Piranha clean is a thin layer isotropic etching and therefore the solution can remove organic residues and particles very proficiently. However, these solutions are not strong enough to remove the saw damage layer or it may take very long time. High concentration of aqueous alkali solutions and acidic solution is therefore used to remove the saw damaged surface. The alkali and acidic solutions isotropically etches the surface and removes the saw damage effectively and leaving the surface smooth and shiny. Furthermore, after completion of the saw damage removal process with these solutions, a square shaped texture appeared on the surface of all the substrate which has been observed initially by optical microscope (see Figure 9.4) and later verified by FE-SEM. Similar observation has been also made by Jongsung and Park *et al.* [22]. The observation obtained further corroborate the hypothesis that high concentration of aqueous alkali or acidic solution causes a square shape textured pattern on monocrystalline silicon surface.

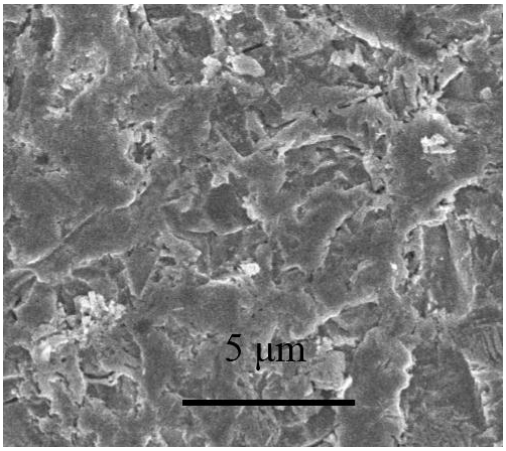


Figure 9.3 Saw-Damaged Surface of As-Cut *P*-Type Monocrystalline Silicon Wafer (Observed by FE-SEM)

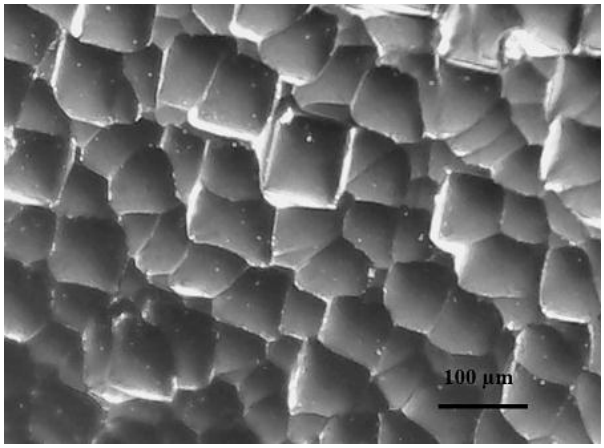


Figure 9.4 Square Shape Pattern (Observed by Optical Microscope)

As stated earlier, the reflectance of different saw damage removed substrate has been measured by using UV-VIS-NIR spectrophotometer. The reflectance curves obtained from spectrophotometer are shown in Figure 9.5. The results obtained from the reflectance curves inferres that for both 10 wt% NaOH and 20 wt% KOH-13.33 wt% IPA solution reflectivity increases with the increase of process time. The lowest reflectance is observed when 10 wt% of NaOH solution has been used for 10 min. The reflectance curve of 10 min NaOH solution has the lowest reflectance. Here, reflectivity lies between 8-3.9% for 250-820 nm wavelength range. It is very closely followed by the 20 min KOH solution reflectance curve where reflectivity lies between 9.1-4.1%. Therefore, it is observed that increasing the concentration

of alkaline or acidic solution or keeping the high concentration constant, while increasing the process time, the reflectivity of as-cut wafer also increases. This is because of the fact that isotropic etching occurs as the time progresses and the surface becomes shinier and smoother. The large square shape pattern observed therefore represents shinier and smoother surface. It is suffice to say here that with appropriate solution and timing an as-cut wafer can be converted into a polished wafer. By using the dial indicator instrument the thickness of the samples has been measured. The dial indicator has been placed in a very flat surface (like glass) so that the contact point touched the flat surface and the pointer arm on the dial indicated zero. Once, the sample is placed under the contact point due to movement of the plunger, the pointer arm rotated clockwise and thickness value of the sample has been obtained. As thickness of the sample is not uniform, several point thickness has been taken and then averaged. It is found that on average the substrate thickness for 10 min NaOH sample and 20 min KOH sample are 173.9 µm and 177.3 µm respectively. However, these findings do not provide any kind of concrete support against wafer thickness and reflectivity.

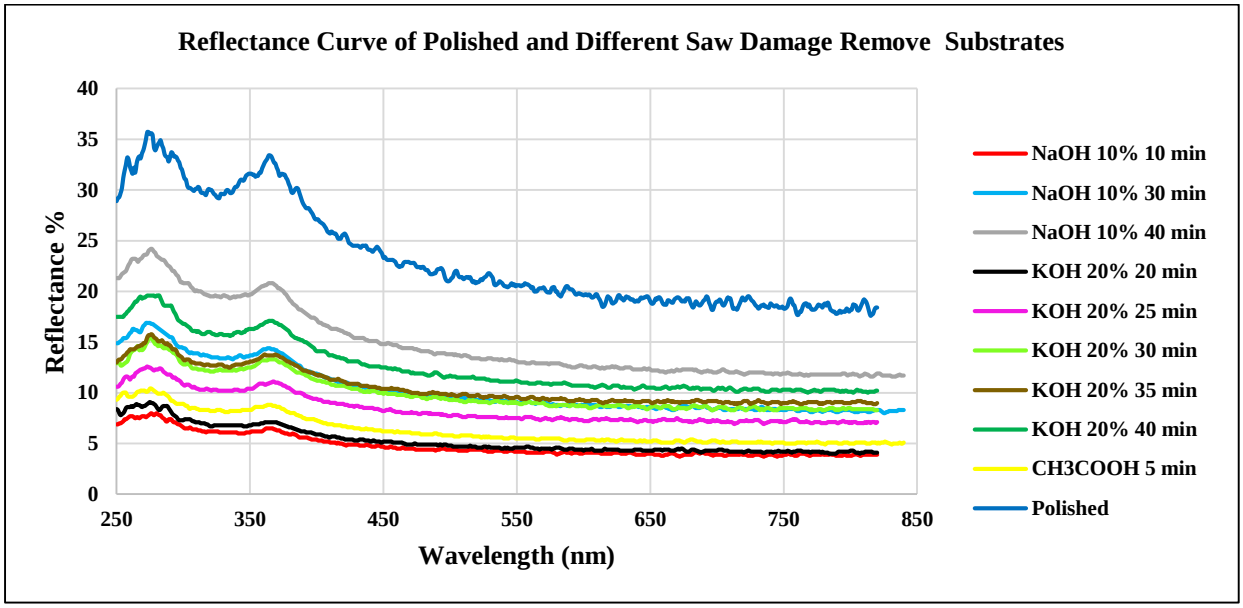


Figure 9.5 Reflectance Curve of Polished and Different Saw Damage Remove Substrates

HF/Nitric/Acetic acid (HNA) is an acidic solution which etches isotropically. By submerging the substrate in HNA solution for 5 min, the substrate becomes shiny. For 250-840 nm wavelength range, the reflectance of the substrate lies between 10.4-5.1%. It is found that by using HNA solution saw damage can also be removed. However, handling HNA solution is difficult than NaOH and KOH solution. Moreover, NaOH price is the lowest among all of these chemicals. Therefore, among all the texturization process 10% NaOH solution for 10 min has been used for saw damage removal process. Four point probe measurement revealed that the sheet resistance of the as-cut substrates lies between 1.12-9.46 Ω.cm. As the doping concentration of the substrate is not uniform, the sheet resistance varies significantly. However, it is observed that the sheet resistance of the substrates lies within similar range after the saw damage removal process has been carried out.

9.3.2 Result of Texturization Process

By using 11.8 wt% Na_2CO_3-1.5 wt% $NaHCO_3$ and 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$ solution in the texturization process, it is observed that reflectivity decreases with the increase of

texturing time while keeping the concentration constant. Moreover, the concentration and duration of the texturization process of this work is in agreement with Sparber et al. [6] who modified the solution recipe used by Nishimoto and Namba [14] where 11.8 wt% Na_2CO_3-1.5 wt% $NaHCO_3$ solution has been used for 40 minutes at 90°C. However, the temperature range used in this work ranges from 70°C to 80°C instead of 90°C in order to keep an option to insert IPA (Isopropyl Alcohol) with this solution in our future work as IPA evaporates ≥ 82.6°C. Between two Na_2CO_3-$NaHCO_3$ solution with different texturization timing, the lowest reflectance is observed while using 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$ solution for 50 min. The reflectance spectra between 250 and 850 nm wavelength are shown in Figure 9.6. The reason for low reflectance is formation of pyramidal microstructures on the surface of the wafer which has been observed by FE-SEM as shown in Figure 9.7. The similar development of low reflectance that occurred due to formation of pyramidal microstructure has been also observed by Ma et. Al. Where 12.84% average reflectivity has been achieved by using 20 wt% Na_2CO_3-4 wt% $NaHCO_3$ solution for 30 min [23].

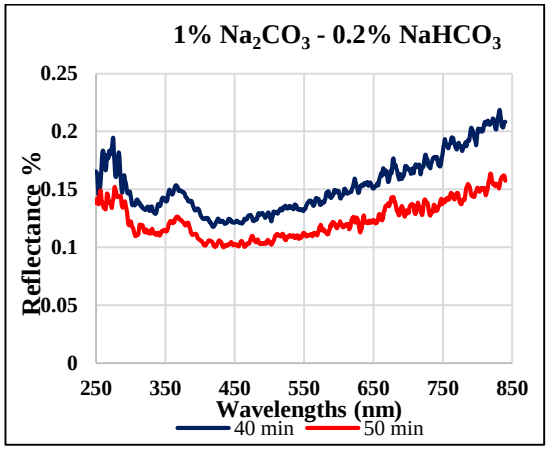


Figure 9.6 Best Reflectance Curves of Na_2CO_3-$NaHCO_3$ Solution

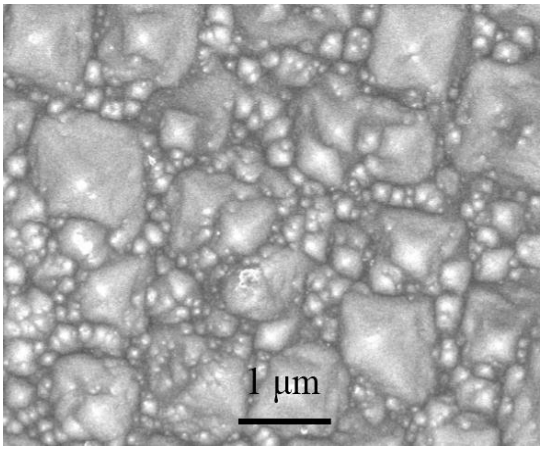


Figure 9.7 Textured Wafer Surface for 50 Min 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$ Solution

The correlation between time and reflectivity is not obvious during texturization with 1.9 wt% KOH-4.7 wt% IPA solution (Figure 9.8) as observed previously using Na_2CO_3-$NaHCO_3$ solution. The lowest reflectance is observed for 20 and 25 min curves. From 250 nm up to about 500 nm wavelength region, lowest reflectivity is found for 20 min of texturization process. On the other hand, lowest reflectivity for 25 min of texturization process is observed between 500 nm and 840 nm wavelength region. The lowest reflectance is measured at 400 nm for both 20 and 25 min texturization process are 0.106% and 0.114% respectively, whereas at 800 nm wavelength the lowest reflectance's for both are ~ 0.05%. Because of negligible difference between 20 min and 25 min reflectance spectra between 500 nm to 840 nm region, it is suffice to say that 20 min of texturization process with 1.9 wt% KOH-4.7 wt% IPA solution has the lowest reflectance curve. Even though the concentration of KOH normally varies from 1% to 5%, the lowest reflectance is found using 0.76 wt% concentration of KOH with 4 wt% IPA solution (see Figure 9.9). The lowest reflectance spectrum is observed for 20 min texturization process, where the absolute reflectance is 0.1-0.026% within 250-800 nm wavelength region. As stated earlier, the base material (as-cut wafer) reflectance is 1.049-0.75% within 250-800 nm wavelength region. So a drastic change is observed in the reflectance and this is due to the texturization process. The reflectance decreases up to 20 min and afterwards it increases with duration of texturization process. Once the saw damage removal

process has been completed, the most interesting aspect of the reflectance spectrums of the substrates with KOH-IPA texturization is that it take 20-25 min time to form proper pyramidal structure with low concentration of KOH-IPA solution. Therefore, the texturization process duration is one of the predominant factor for reduction of reflectivity. Moreover, due to change in density and height of the pyramids the reflectivity may vary [24-25]. Other factors which may influence the reflectivity character include temperature and concentration of the solution used [26].

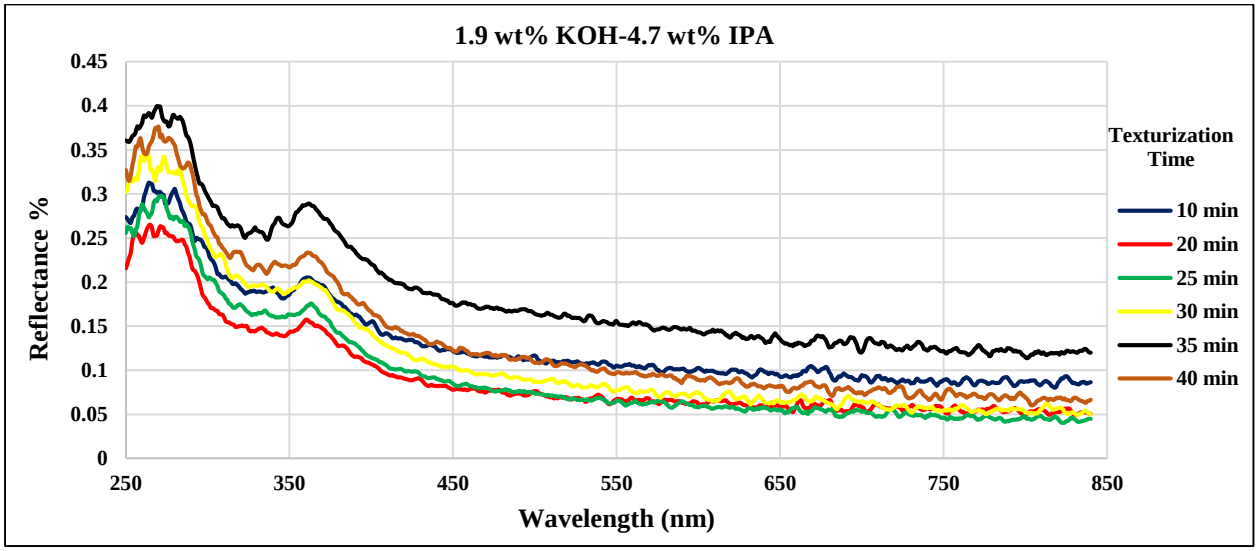


Figure 9.8 Reflectance Curves of Textured Substrate

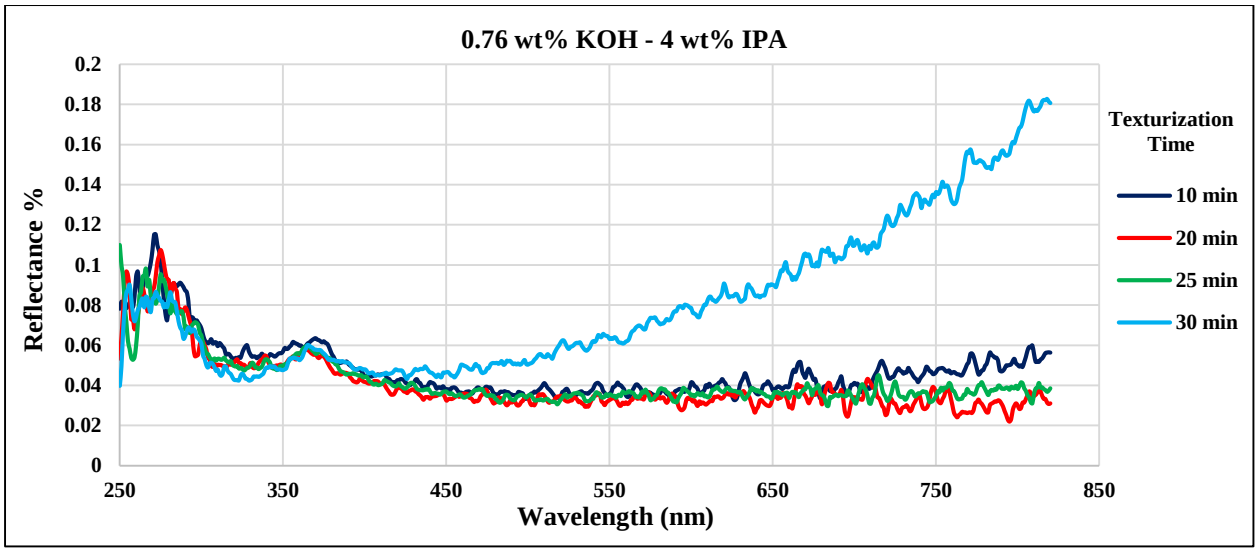


Figure 9.9 Best Reflectance Curves of Substrate Textured in 0.76 wt% KOH-4 wt% IPA Solution

In all the cases of texturization process, pyramidal microstructures are formed on the silicon surface. There are different theories about how the pyramidal microstructures are formed. However, the most concurring point in all the theories is that there is a masking agent in the wet chemicals used in texturization process which locally prevents silicon from being etched, while non-masked areas are etched until {111} planes are exposed and forms pyramids upon the surface of (100) silicon [27-29]. In this work, it is found that 20 min textured wafer has the lowest reflectance, because of proper formation of pyramidal microstructures on the surface of

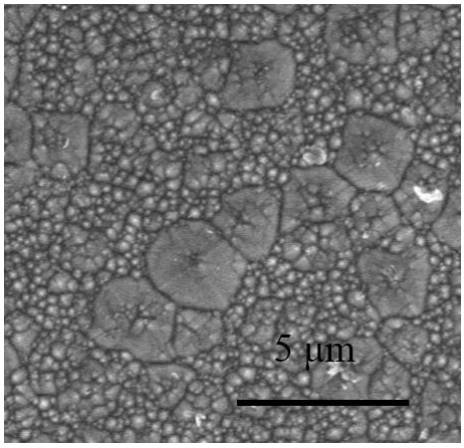


Figure 9.10 (a) 10 Min, (Top View)

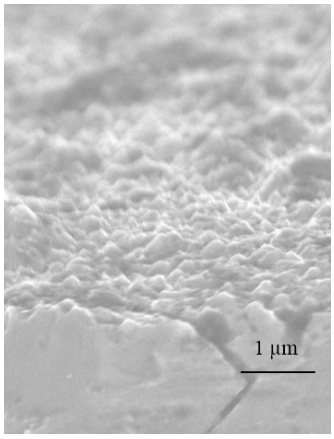


Figure 9.10 (b) 10 Min, (Side View)

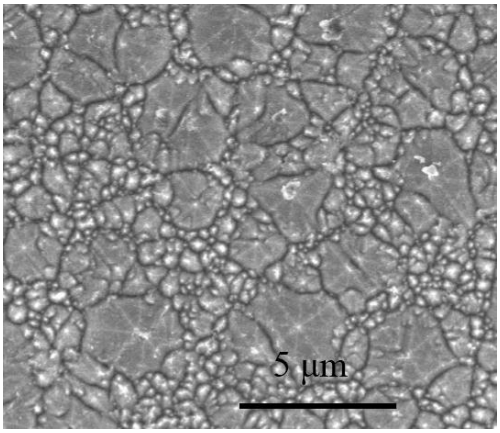


Figure 9.11 (a) 20 Min, (Top View)

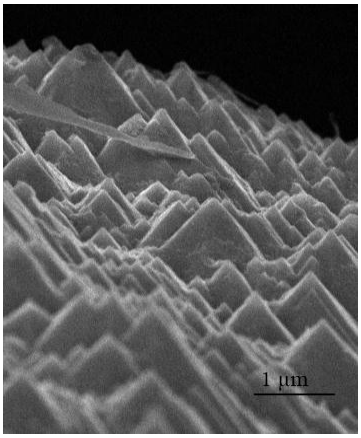


Figure 9.11 (b) 20 Min, (Side View)

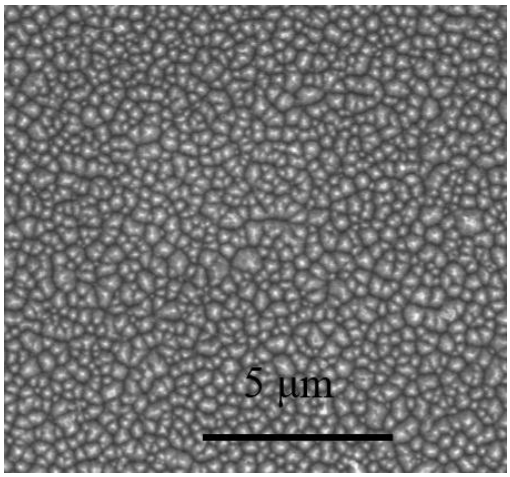


Figure 9.12 (a) 30 Min, (Top View)

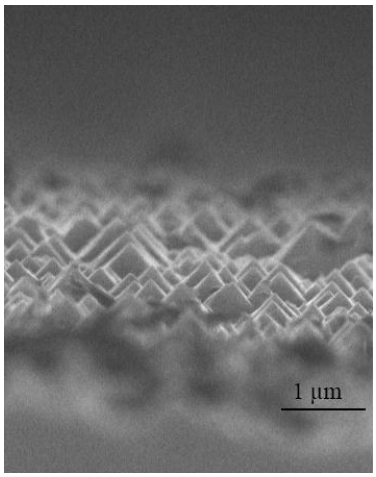
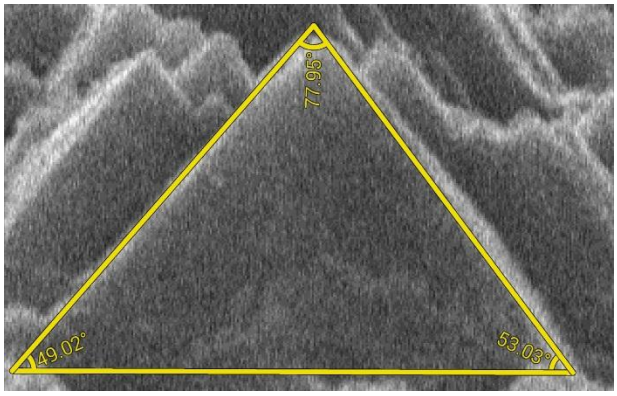


Figure 9.12 (b) 30 Min, (Side View)

the silicon wafer. Comparing the pyramidal structure as observed in Figure 9.10 (10 min textured), the one with 20 min textured wafer (Figure 9.11) has many big pyramids and few small pyramids. Here pyramids are properly formed and that is why the reflection is found lowest for 20 min texturing. Interestingly, with further increase of texturization time (e.g. 30 min), the pyramids again are getting smaller in size as shown in Figure 9.12(a) and 9.12(b) and therefore the reflectivity decreases.



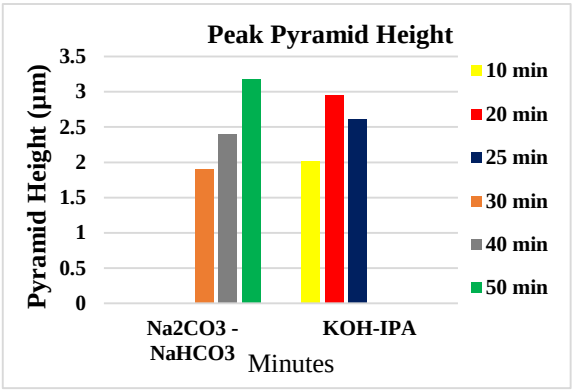
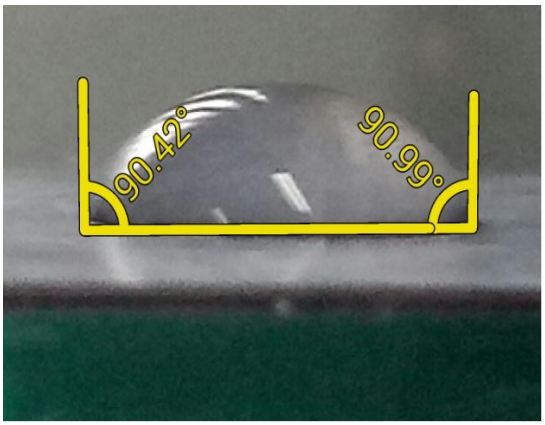


Figure 9.13 Pyramid Angles

Figure 9.14 Pyramids Height

The pyramid angles of the lowest reflectance textured substrate are measured using image meter software. It is found that most of the pyramids consist of acute triangles. Figure 9.13 shows the pyramid having acute angles 77.95°, 49.02° and 53.03°. However, in some cases obtuse triangle (91.71°, 36.85° and 51.44°) has been also observed. The height of the peak of the pyramids of the textured wafer has been measured using Brukar DektakXT stylus surface profilometer. Measurement shows (Figure 9.14) that the height of the pyramid lies between 1.75 µm to 3.20 µm [30]. It is also observed from Figure 8.14 that there is a relation between the peak height of the pyramid and the reflection property. The highest pyramid has the lowest reflectance which is true for both (0.76 wt% KOH-4 wt% IPA and 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$ solution) textured substrates. However, reflectivity does not depend only on the height of the pyramids but also on the number of pyramids in a given area and angle of the pyramids. Contact angle determines whether a surface is hydrophilic or hydrophobic. Again, by using image meter software, contact angle of the textured wafer has been determined as shown in Figure 9.15. Contact angle measurement shows that angle is slightly greater than 90°. Therefore, the surface falls in the nearly-hydrophobic to hydrophobic range [31].



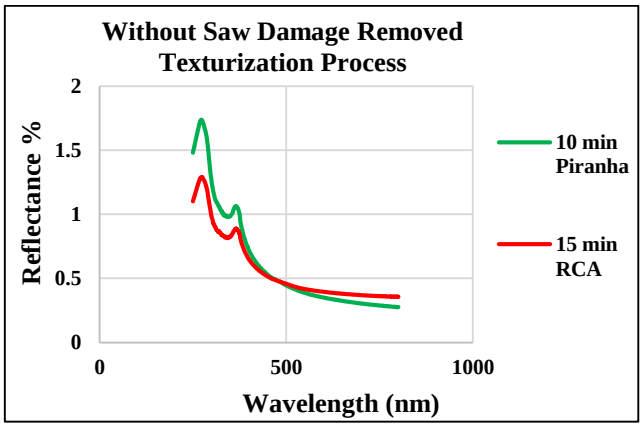


Figure 9.15 Contact Angles

Figure 9.16 Reflectance Curves

Texturization process with 1 wt% TMAH-4 wt % IPA solution for 20 min and 40 min at 80°C did not show any significant improvement of reflectance. As stated earlier, after cleaning the substrates with RCA-1 and Piranha solution separately, texturization has been done without saw damage removal process with 0.76 wt% KOH-4 wt% IPA solution and with various time duration at 70°C to 80°C. Result shows that 15 min RCA clean textured wafer has the lowest reflectance among 10, 15 and 25 min RCA cleaned texturization process. Whereas, 10 min

Piranha clean textured wafer has the lowest reflectance among 10, 20, 25 and 30 min Piranha cleaned texturization process. Figure 9.16 shows the best overly reflectance spectra obtained from RCA and Piranha cleaned texturization process. However, the lowest reflectance still observed for saw damaged removed substrate textured in 0.76 wt% KOH-4 wt% IPA solution for 20 min. All the textured surface sheet resistance lies within the range as mentioned earlier in section 9.3.1. Like saw damage removed substrates sheet resistance, the specific sheet resistance value of textured substrate could not be measured.

Figure 9.17 Different Silicon Wafers with Different Colour

Figure 9.17 shows colour variations of different wafers used in this experiment. Initially the as-cut wafers are gray in colour. After removing the saw damage, wafer becomes very shiny and white in colour. The wafers become near black in colour after texturing with 0.76 wt% KOH-4 wt% IPA solution. In general, it is known that white object reflects more light and black object absorbs more light. So by visual observation it can be also concluded that textured wafer absorbs more light than as-cut or saw damage removed wafer.

9.4 Summary

In this research, considering as-cut monocrystalline silicon wafer as base material different concentrations of Na_2CO_3 and $NaHCO_3$ solution, KOH-IPA solution and TMAH solution with varied time intervals has been investigated for texturization process and discussed in this chapter. Furthermore, saw damage removal process has been conducted with 10% NaOH solution, 20 wt% KOH-13.33 wt% IPA solution and HNA solution. FE-SEM and optical microscopy confirms the formation of square shaped pattern. Depending on time, cost and reflectivity 10% NaOH solution shows the most promising result and has been used in prior arts for the texturization process. Different texturization process outcome indicates absolute reflectance of 0.1-0.026% within 250-800 nm wavelength region can be achieved by using 0.76 wt% KOH-4 wt% IPA solution for 20 min. It should be mentioned that the base material is as-cut monocrystalline silicon wafer and the base material reflectance is 1.049-0.75% within 250-800 nm wavelength region. The reduction of base material reflectance is because of the formation of proper pyramidal microstructure on the surface of silicon wafer during texturization process. These pyramidal microstructure formation have been observed via FE-SEM. Measurement shows that the height of the pyramid on the silicon surface varies from 1.5 µm to 3.18 µm and inclined planes of the pyramids are acute angle. Contact angle being slightly above 90° indicates that the textured wafers surface falls in the near hydrophobic to hydrophobic range. It is observed that an alternative to 0.76 wt% KOH-4 wt% IPA solution is the use of 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$ solution for 50 min. Reflectance measured for this

solution is not as low as 0.76 wt% KOH-4 wt% IPA solution but still the textured substrate absolute reflectance is very low within 250-800 nm wavelength region and the chemicals used in this process are less harmful and much safer to handle. As wet chemical processing can be scaled up with low manufacturing cost and at the same time the texturization recipes (0.76 wt% KOH-4 wt% IPA or 1 wt% Na_2CO_3-0.2 wt% $NaHCO_3$) yields very low absolute reflectance within 250-800 nm wavelength region, any of these texturization process can be used in monocrystalline silicon solar cell fabrication process to reduce reflectivity and enhances light absorption.

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Chapter 10

FORMATION OF *N*-TYPE LAYER USING $POCL_3$ DIFFUSION

10.1 Introduction

Since the discovery of the *P*-*N* junction by Russell Ohl in 1940 [1], science has come a long way. Moreover, the application of *N*-type layer upon *P*-type layer has huge impact, not only on silicon solar cells as the emitter layer but also in microelectronics industry [2]. A *P*-*N* junction can be fabricated by creating an *N*-type layer upon a *P*-type layer with donor implantation or diffusion technique [3]. Although, there are various techniques to create an *N*-type layer upon a *P*- type layer, this chapter discuss about the formation of *N*-Type layer (Emitter) over monocrystalline *P*-type silicon wafer (Base) using $POCl_3$ (Phosphorus Oxychloride) diffusion. Furthermore this chapter also discuss about, required temperature, gas, APCVD chamber etc. which are needed for $POCl_3$ diffusion technique.

10.2 Background Study

10.2.1 Thermal Diffusion

Doping refers to the addition of specific impurities to a semiconductor to modify its electrical properties. Moreover, there are two main methods of doping [4]. They are, thermal diffusion and ion implantation. In this work, thermal diffusion has been used. Hence, only thermal diffusion is discussed in this chapter. Generally thermal diffusion is a two-step process [4],

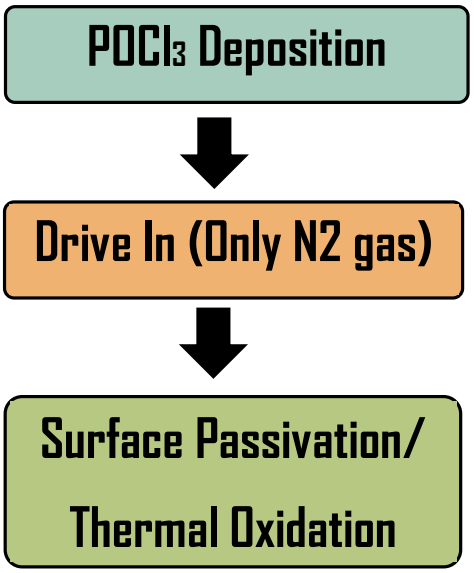


Figure 10.1 Stages of Diffusion Process

i. Deposition / Pre-deposition: dopant atoms are introduced at the wafer surface.

ii. Drive-in: the dopant atoms then diffuse into the wafer to create the required concentration gradient.

However, a third step called surface passivation-/ thermal oxidation has been included for diffusion the thermal diffusion process. It is well known that, high surface recombination rate reduces short circuit current and thus the efficiency of solar cells. The surface recombination of photo-excited electron-hole pair takes place because of the dangling bonds at the top of surface. By reducing the number of dangling bonds surface recombination can be lowered. Generally, a technique called thermal oxidation is used to reduce the surface recombination. In thermal oxidation technique a "passivating" layer is grown thermally. The surface passivating layer is fabricated with silicon oxide (SiO_2) which is used to passivate the surface. By applying only O_2 gas SiO_2 layer can be grown upon Si_3N_4 layer [5]. All the thermal diffusion steps are shown in Figure 10.1.

10.2.2 Chemical Vapor Deposition (CVD)

Thermal diffusion can be performed with chemical vapor deposition technique / equipment. Chemical vapor deposition is a process, where gaseous reactants can be deposited onto a substrate [6]. There are several types of CVD, including low pressure chemical vapor deposition (LPCVD), atmospheric pressure chemical vapor deposition (APCVD), metal-organic chemical vapor deposition (MOCVD) etc. [7].

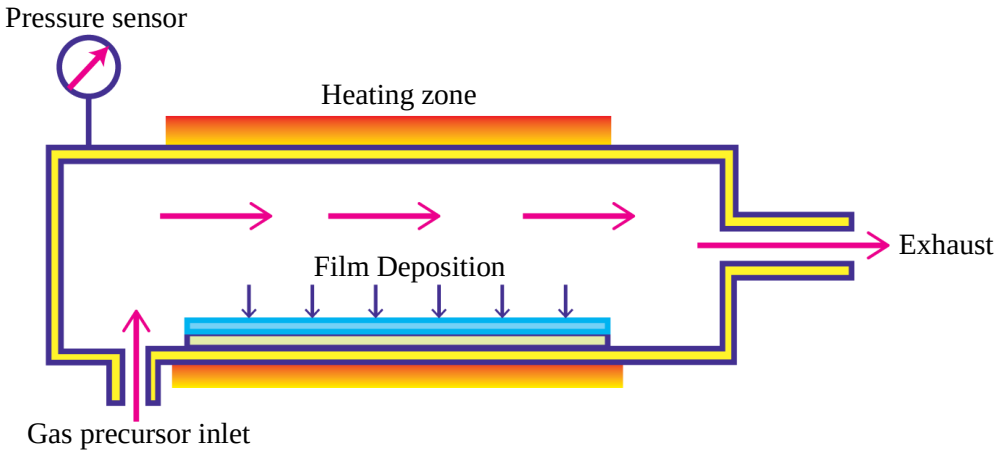


Figure 10.2 Simple CVD Reactor [8]

Figure 10.2 shows a simple CVD reactor. Where, precursor gases (often diluted in carrier gases) are transported into the reaction chamber normally at high temperature. When the gas pass over or come into contact with a heated substrate, reaction or decomposition take place, thus formation of a solid phase happens, which are then deposited onto the substrate. Here in this work, an APCVD chamber has been used.

10.2.3 $POCl_3$ diffusion furnace

N_2 gas (carrier gas), O_2 gas and liquid Phosphorous Oxicloride ($POCl_3$) have been used in a $POCl_3$ diffusion furnace to create *N*-type layer upon *P*-type layer. Furthermore, the flow meters of $POCl_3$ diffusion furnace is adjusted to 14.7 psi (1 atm) to operate it as an APCVD chamber. The schematic diagram of the gas distribution system of $POCl_3$ furnace is shown in Figure 10.3 and the $POCl_3$ diffusion furnace is shown in Figure 10.4.

Here nitrogen being an relatively inert gas, not only, nitrogen purge provides an inert environment before the drive-in process (pre-deposition) for contamination and moisture-free diffusion chamber but also purges the reactive gases after the completion of a process [9]. This contamination eradication process is known as 'nitrogen purge'. Also N_2 gas (carrier gas) serves as a medium for transporting phosphorus molecule which will be deposited upon *P*-type layer in the drive-in stage.

During deposition stage, the carrier N_2 gas flows through a 2000cc bubbler, filled with liquid Phosphorous Oxicloride ($POCl_3$) to produce gaseous $POCl_3$. The gaseous $POCl_3$ vapor is needed for phosphorous deposition in the deposition stage. During deposition stage, the carrier O_2 gas also flows. Oxygen gas reacts with $POCl_3$ vapor to create P_2O_5 film in the deposition stage, which is necessary to form phosphorous layer upon *P*-type wafer.

Surface passivation is necessary for low recombination rate [10], which is, reduction of dangling bonds in the surface layer. Surface passivation is done using thermal oxidation technique which actually forms SiO_2 layer upon surface. So, to form silicon dioxide layer O_2 gas has been used in O_2 soak step. O_2 soak step also known as surface passivation step happens after drive-in process.

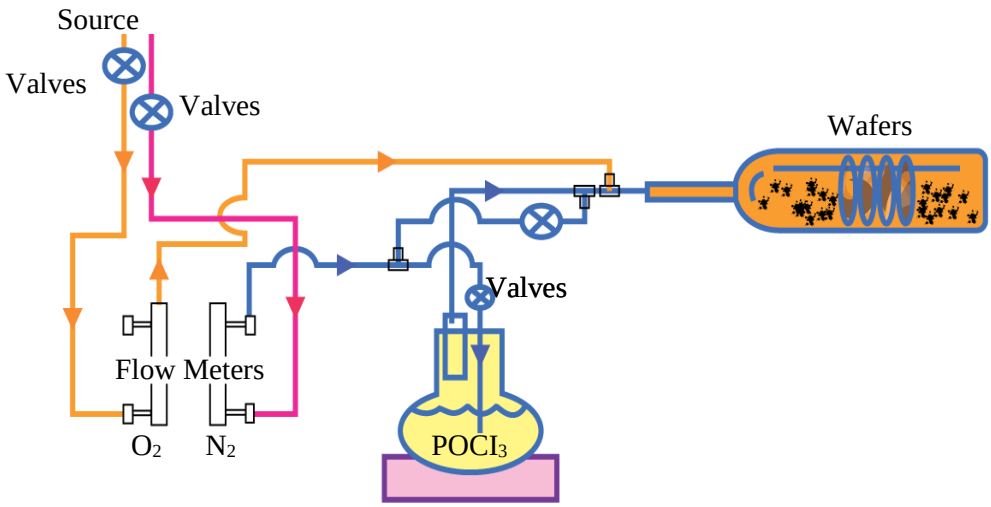


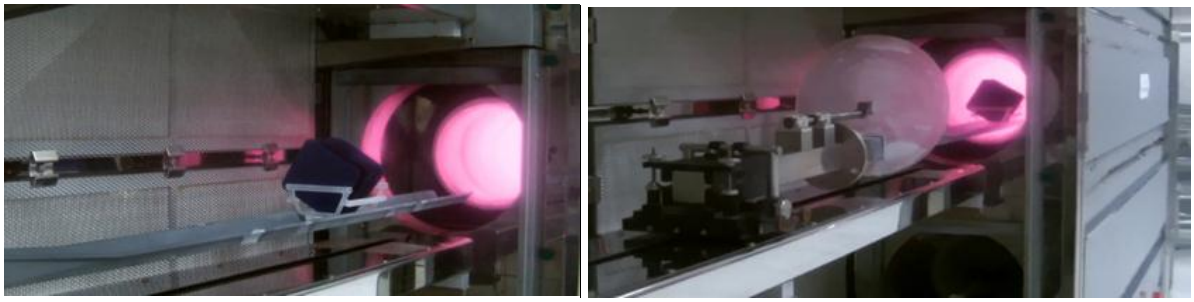
Figure 10.3 Schematic Diagram of the Gas Distribution System of $POCl_3$ Furnace

Figure 10.4 $POCl_3$ Diffusion Furnace

10.3 Experimental

10.3.1 Operation and Process Time

At first, the $POCl_3$ furnace system is turned on. When the chamber temperature reaches 200°C, N_2 purge is turned on to have an inert environment, contamination and moisture-free diffusion chamber. After reaching 700 °C, the wafers are loaded into the chamber as shown in Figure 10.5.



(a) (b)

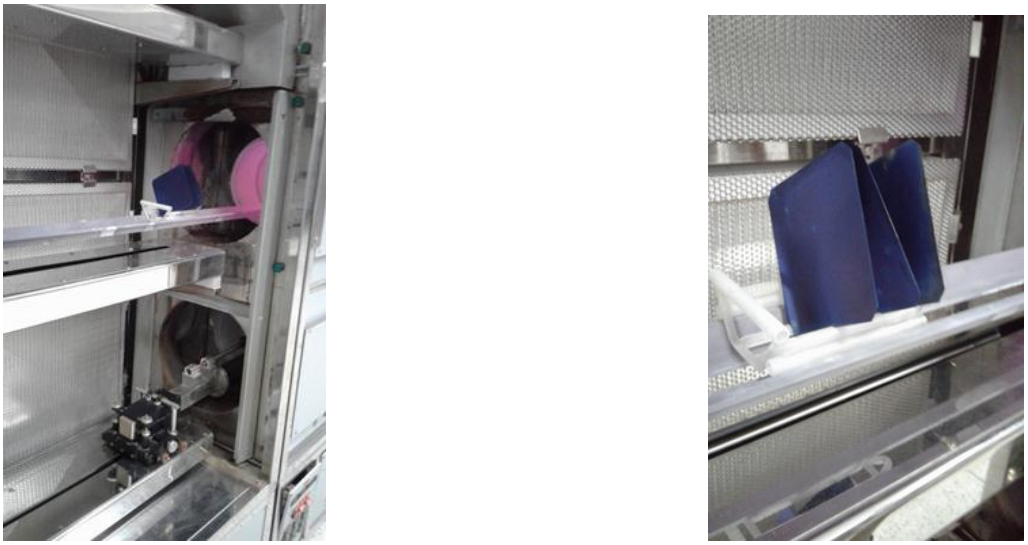
Figure 10.5 Insertion of Wafer into the Furnace

Subsequently reaching 875°C, to start the deposition process, N_2 purge has been turned off and N_2 source and O_2 source are turned on for 5 min. It should be mentioned that, N_2 source is connected liquid $POCl_3$ bubbler, N_2 gas reacts liquid $POCl_3$ thus creating gaseous $POCl_3$, so actually $POCl_3$ vapor will go to the chamber. Moreover, N_2 and O_2 gas flow rate is adjusted to 14.7 psi (Pounds per square inch) to have an atmospheric environment. After 5 min, N_2 and O_2 source are turned off by setting the flow meter to zero, and N_2 purge has been turned on for 10 min for drive-in process. After completion of drive in process N_2 purge has been turned off and O_2 source are turned on for 10 min for surface passivation. Again, after surface passivation O_2 source are turned off and N_2 purge is turned to for 10 min, to have inert environment, contamination and moisture-free diffusion chamber. During last N_2 purging, the temperature is lowered to 700°C and the wafers are pulled out from the chamber (Figure 10.6). Lastly, the temperature is lowered to 200 °C and the system is turned off. The wafers are cooled down for 30 min. During the operation, the flow rate of N_2 and O_2 are 200 sccm. The process steps and timeline is shown in Table 10.1 and Figure 10.7.

TABLE 10.1: Steps of Diffusion Process

Step	Name	Time	Temp.	Gas
0	**Idle**	**0**	**200**	**-**
1	**Wafer Load**	**23**	**700**	**N_2 Purge**
2	**$POCl_3$ Deposition**	**50**	**875**	**N_2 & O_2 & $POCl_3$**
3	**Drive In**	**55**	**875**	**N_2Purge**
4	**Surface Passivation**	**65-75**	**875**	**O_2**

5	**Wafer Out**	**105**	**700**	**N_2 Purge**
6	**Idle**	**120**	**200**	**-**



(a) (b)

Figure 10.6 (a) Doped Wafer Unloading From Furnace (b) Phosphorus Doped Wafer

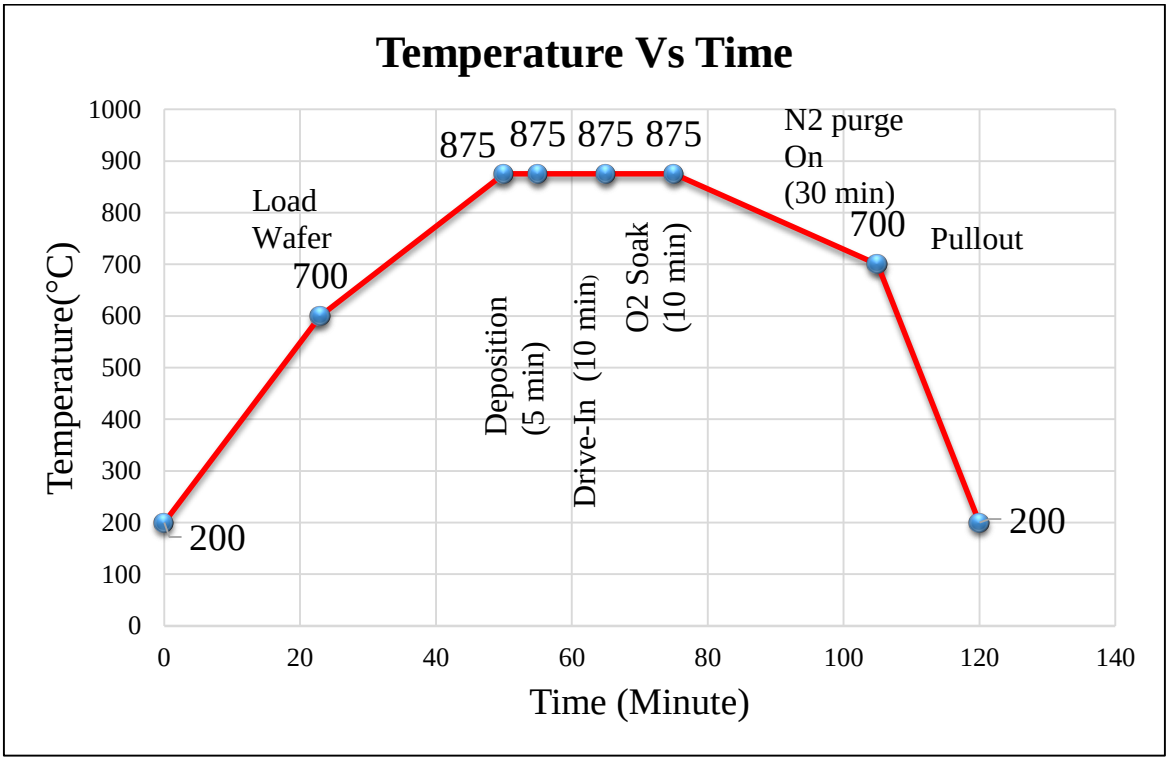


Figure 10.7 Temperature and Timing Graph of Diffusion Process

The whole process has been done several times with varying deposition and drive time. The deposition and drive-time are 5 min-10 min, 10 min-15 min, 15 min-20 min, 20 min-25 min, 20 min-25 min and 25 min-30 min respectively.

10.4 Results and Discussion

To form *N*-type layer using $POCl_3$ thermal diffusion technique, a 12.5×12.5 cm^2, thickness 200 µm , monocrystalline *P*-type wafer is used. By using four point probe method the calculated sheet resistivity is found 2.3 Ω-cm or 114.81 Ω/□ for the *P*-type wafer. After *N*-type layer is formed, the sheet resistance is found 65.25 Ω/□ for 5 min diffusion and 10 min drive-in. Sheet resistance determination process is discussed in details in chapter 11. As solar cell sheet resistance lies between 60-100 Ω/□. Also depending on time, sheet resistance, carrier concentration and cost 5 min diffusion and 10 min drive time is considered as optimum diffusion recipe.

Hot probe method can determine whether it is a *P*-type (by showing negative voltage) or *N*-type wafer (by showing positive voltage) and can also determine the doping uniformity profile [11-12]. A simple hot probe test has been done and all the cases it is seen that *N*-type layer is formed upon *P*-type wafer. Details of hot probe method is discussed in chapter 11. The *N*-type layer is formed upon *P*-type wafer because of reaction between different gases. Generally, phosphorous diffusion process is performed in two steps. The first step is called deposition that involves the formation of phosphorous-rich oxide films on the silicon substrate.

TABLE 10.2: Sheet Resistance of Doped Wafer

Diffusion Time	Drive In Time	Sheet Resistance (Ω/□)
5min	10 min	65.25
10min	15 min	44.62
15min	20 min	13.53
20min	25 min	32.75
30min	35 min	55.38

At first, Nitrogen gas flows through liquid Phosphorous Oxicloride and thus producing Phosphorus Oxychloride vapor, which reacts with oxygen and forms Phosphorus Pentoxide. The reactions are shown in the following equations [13- 14]:

$$\mathbf{POCl_3\ (liquid) + N_2\ (bubble) \rightarrow POCl_3\ (vapor)\ (pre-deposition)}$$

$$\mathbf{4POCl_3\ (vapor) + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2}$$

The second step is called drive-in where the phosphorous-rich oxide film acts as an infinite source for phosphorous diffusion into the Si substrate. The P_2O_5 immediately reacts with the silicon, by resulting in, in-diffusion of phosphorus and formation of the phosphosilicate glass (PSG). The phosphosilicate glass is normally etched off using dilute hydrofluoric acid, but has been not done in this case. By applying O_2 gas in the surface passivation stage the SiO_2 layer has been grown upon phosphosilicate glass (PSG). Rest of the reactions are given below

$$\mathbf{2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2\ (drive\text{-}in)}$$

$P + 3Si \rightarrow n-$ type doped Si

Although for $POCl_3$ thermal diffusion technique large amount of N_2 and O_2 gases are needed to complete the whole processes, for commercial purpose, $POCl_3$ thermal diffusion technique is a better process than spin coating or dip coating of P_5O_9 dopant solution. Furthermore, if the wafer size is large, and good doping uniformity is required for large scale production than $POCl_3$ thermal diffusion technique is the better technique than P_5O_9 dopant solution.

10.5 Summary

In this chapter, the formation of *N*-Type layer over monocrystalline *P*-type silicon wafer using $POCl_3$ thermal diffusion technique has been discussed. Sheet resistance measurement using four point probe and hot probe test shows that, in all the cases *N*-type layer has been formed upon the *P*-type monocrystalline silicon wafer. The sheet resistance has been found 65.25 Ω/□ for 5 min diffusion and 10 min drive-in. As solar cell sheet resistance lies between 60-100 Ω/□. Also depending on time, sheet resistance, carrier concentration and cost 5 min diffusion and 10 min drive time is considered the optimum diffusion recipe. It is seen that for large scale production of large wafers, with good doping uniformity $POCl_3$ thermal diffusion technique provides the minimum cost. Thus it can be said that, $POCl_3$ thermal diffusion technique is a good technique and can be used commercially for the formation of *N*-Type layer over monocrystalline *P*-type silicon wafer.

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Chapter 11

CHARACTERIZATION OF SOLAR CELL AND DIFFERENT SILICON WAFER

11.1 Introduction

Characterization refers to a process by which a material's structure and properties are probed and measured. In materials science, the word characterization involves knowing any physical, mechanical or chemical properties of a material [1]. Characterization is needed to understand the behavior of material and it helps to improve and explain the parameters of a material. In this chapter, characterization process of different silicon wafer and solar cell has been explained. Also characterized parameter values are mentioned.

11.2 Characterization

While there are many characterization techniques here only these techniques that are used to characterize solar cell and different silicon wafer, have been discussed.

11.2.1 Thickness Measurement

Thickness measurement has been done using dial indicator instrument. Details about dial indicator has been discussed previously in chapter 3, section 3.3. It is seen that, the thickness of a *P*-type pseudo-square mono-crystalline silicon wafer used in Bangladesh is in the range of 180 to 200 μm. Although the specification says the thickness the *P*-type pseudo-square mono-crystalline silicon wafer is 200 μm ± 20 μm, no wafer is found whose thickness is greater than 200 μm.

After saw damage removal process it is found that, on an average the substrate thickness for 10 min NaOH sample and 20 min KOH sample are 173.9 μm and 177.3 μm respectively (see details in chapter 9 section 9.3.1).

11.2.2 Microscopy Analysis

The microscope is an extremely useful instrument in the examination of a material. Microscopy allows us to obtain images from objects that cannot be seen with the unaided eyes. The three main branches of microscopy analysis are optical, electron, and scanning probe microscopy [2]. For optical microscopy, here, total four types of optical microscopes have been used to inspect the surface morphology of different types of silicon wafer and busbars and grid fingers of solar cell. AmScope digital trinocular stereo microscope (Figure 3.5 (a)) has been used in this research for busbars and grid finger analysis. The resolution capability of this microscope is poor. On the other hand to investigate the surface morphology of raw, saw damaged removed and textured wafer are Micros Square, DS-600, Digital Microscope (U1000X) Model: TOL-00067 and ZEISS Stemi 508 microscope with axiocam 105 microscope camera (Figure 3.5 (b, c, d)) have been used. With all these microscopes the surface morphology of raw, saw damaged removed can be well inspected. However Scanning Electron Microscope (SEM) is required to see the surface morphology of textured wafer. It is seen that, the surface of raw and saw

damaged removed wafer are rough and smooth respectively. Square shape pattern has also been observed in saw damaged removed wafer using these microscope.

In this research, for electron microscopy a JEOL JSM-7600F FESEM has been used (Figure 3.12) to investigate the surface morphology of different textured silicon samples. Surface morphology investigation shows that pyramidal microstructure are formed on the surface of silicon wafer during texturization process. All these pyramidal microstructure formation are observed via FE-SEM. (see details in chapter 9 section 9.3).

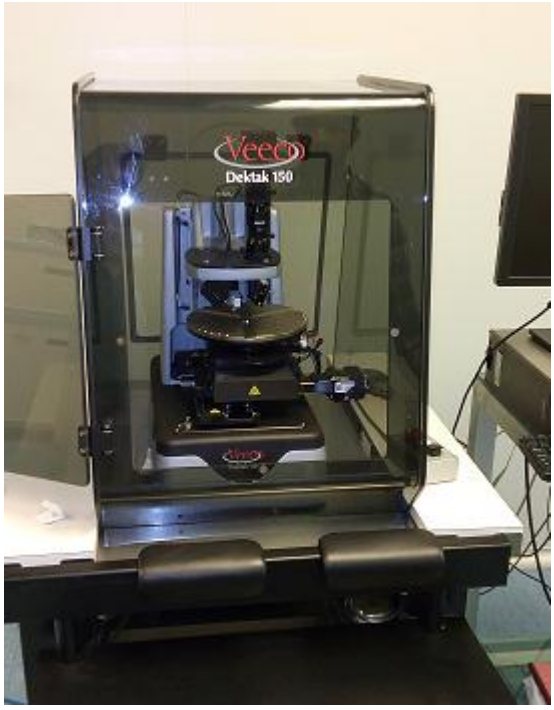

Figure 11.1 Dektak 150 Surface Profiling System

In this research, for scanning probe microscopy surface profilometer has been used. Surface profilometer or surface profiling system is an instrument used to measure the roughness of a surface [26]. In a surface profiling system, a stylus runs along the sample surface and the up-and-down movements of the stylus are measured. Here, a Dektak 150 surface profiling system has been used to (Figure 11.1) measure the grid- fingers surface height uniformity. Surface profilometer measurement tells us that the surface of raw wafer is rough. Furthermore, measurement shows the maximum height of the standard solar cell grid-fingers are 10 µm. Moreover, the width of grid-fingers are 180 micrometer and aspect ratio which is defined as the height to width ratio is 0.0556 for the standard solar cell. On the other hand, it is seen that maximum height of the grid-fingers are 23 µm, width is 500 µm and aspect ratio is 0.046 µm for locally made solar cell. (see details in chapter 5 section 5.2.10). Measurement also shows that the height of the pyramid on the textured silicon surface varies from 1.5 µm to 3.18 µm.

11.2.3 Spectroscopy

Spectroscopy is the branch of analysis that uses the interaction of energy with a sample to perform an analysis that can provide information on the chemical composition and conformation of the samples [3]. From spectroscopy data the physics and behavior of samples can be understand. The spectroscopy is based on the dispersion of light into its component

wavelengths (i.e. energies). The data that is obtained from spectroscopy is called a spectrum. A spectrum is a plot of the intensity of energy detected versus the wavelength (or frequency, etc.) of the energy and provides information on the structure of the sample under analysis. The spectrum is comprised of data across many wavelengths (frequencies, variables), and it is studied so that information can be extracted from the spectral data.

A spectrometer is used in spectroscopy. Here, two types of spectrometer has been used in this research. They are spectral response measurement system and UV-VIS-NIR spectrophotometer.

11.2.3.1 Spectral response measurement system

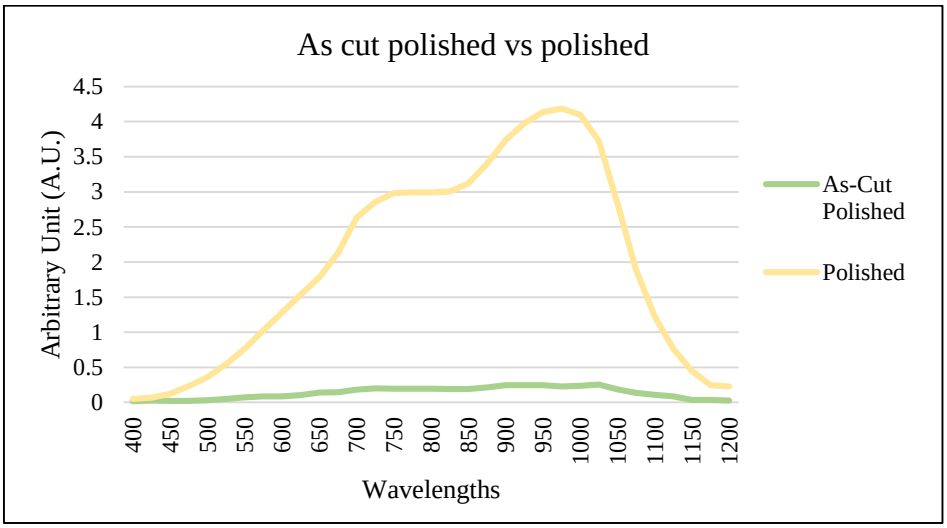

Figure 11.2 Spectral Response of a Polished Side of As-Cut Polished and a Polished Silicon Wafer

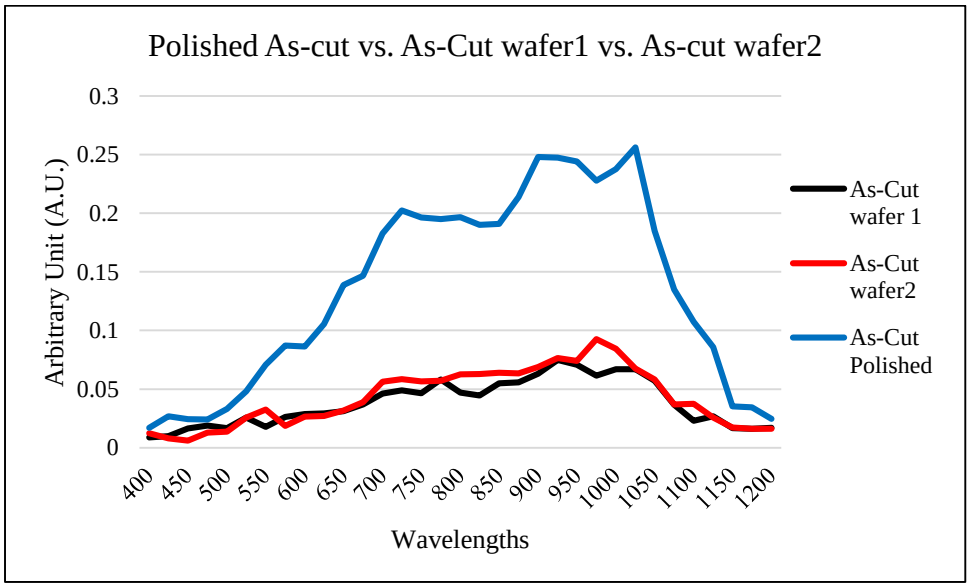

Figure 11.3 Spectral Response of a Polished Side of As-Cut Polished and Two As-Cut Wafer

As sated earlier (chapter 8 section 8.2) spectral response measurement system measures relative reflectivity of a material. Although the system does not give actual reflectivity values, still the system can be used to compare reflectivity between different samples. Here spectral response

hence relative reflectivity of various *P*-type silicon wafer has been observed. Figure 11.2 visualizes the spectral response of the polished side of an as-cut polished and a polished silicon wafer. Depending upon the surface condition of the monocrystalline silicon, the wafer is categorized as both side polished (also known as polished), both side as-cut (also known as as-cut) wafer and as cut polished (one side polished and one side as-cut) wafer. From the spectral response in Figure 11.2 it can be concluded that the reflectivity of the polished side of as cut polished wafer is lower than the polished silicon wafer.

Figure 11.3 visualizes the spectral response of the polished side of an as-cut polished and two as-cut wafer. From the spectral analysis it is clear that the polished side of as cut polished wafer gives higher reflectivity than the as-cut silicon wafers. The spectral response and the reflectivity of the as-cut silicon wafers are almost same.

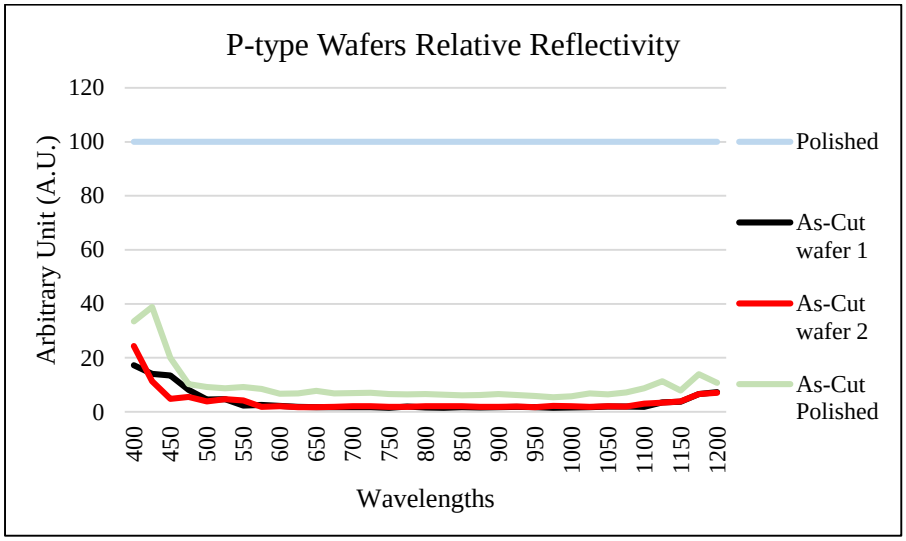

Figure 11.4 Relative Reflectivity Curves (Polished, Polished Side of As-Cut Polished and Two As-Cut Wafer)

From the spectral response the relative reflectivity can be measured. To find out the relative reflectivity from the spectral response a reference must be considered at first. For reference here, the reflectivity of polished *P*-type wafer is considered. Then comparing the other wafers the relative reflectivity graph is obtained that is shown in Figure 11.4. The summary of Figure 11.4 is relative reflectance can be measured and as-cut polished wafer has higher reflectance than as-cut wafers.

11.2.3.2 Ultraviolet-Visible-Near Infrared (UV-VIS-NIR) spectrophotometer

The Ultraviolet-Visible-Near Infrared (UV-VIS-NIR) spectrophotometer measures absolute reflectivity. In this work, the absolute reflectivity of all the samples have been measured by a Hitachi UH4150 (ultraviolet-visible-near infrared) UV-VIS-NIR spectrophotometer. (Chapter 9 section 9.2 and chapter 3 section 3.13 give description.) It is seen that the absolute reflectance for polished wafer using spectrophotometer e is in the range of 37.1-19.7% (Figure 9.1) within 250-800 nm wavelength region. Whereas, for as-cut wafer the reflectance is very low and lies in between 1.049-0.75% (Figure 9.2) within 250-800 nm wavelength region. Once, the saw damage removal process has been done upon as-cut wafer it is seen that reflectance increases. The reflectance curve of 10 min NaOH solution shows that the reflectivity lies between 8-3.9% for 250-820 nm wavelength range. It is very closely followed by the 20 min KOH solution

reflectance curve where reflectivity lies between 9.1-4.1%. All textured wafer has low reflectance than non-textured wafer. Different texturization process outcome indicates absolute reflectance of 0.1-0.026% within 250-800 nm wavelength region which can be achieved by using 0.76 wt% KOH-4 wt% IPA solution for 20 min.

11.2.4 *N*-type and *P*-type determination

The "hot-probe" experiment provides a very simple way to distinguish between *N*-type and *P*-type semiconductors using a soldering iron and a standard multimeter [4]. When applying the probes to *N*-type material, a positive current reading is found on the meter, while *P*-type material gives a negative current.

A voltmeter (or an ammeter) is attached to the sample, and a heat source, such as a soldering iron, is placed on one of the leads. The heat source will cause charge carriers (electrons in an *N*-type, holes in a *P*-type) to move away from the lead. The heat from the probe creates an increased number of higher energy carriers which then diffuse away from the contact point. This will cause a current/voltage difference. For example, if the heat source is placed on the positive lead of a voltmeter attached to an *N*-type semiconductor, a positive voltage reading will result as the area around the heat source/positive lead becomes positively charged. Figure 11.5 shows the hot-probe experiment. All the *P*-type wafers show negative voltage reading in the multimeter and all diffused wafers (*N*-type) show positive voltage reading in the multimeter.

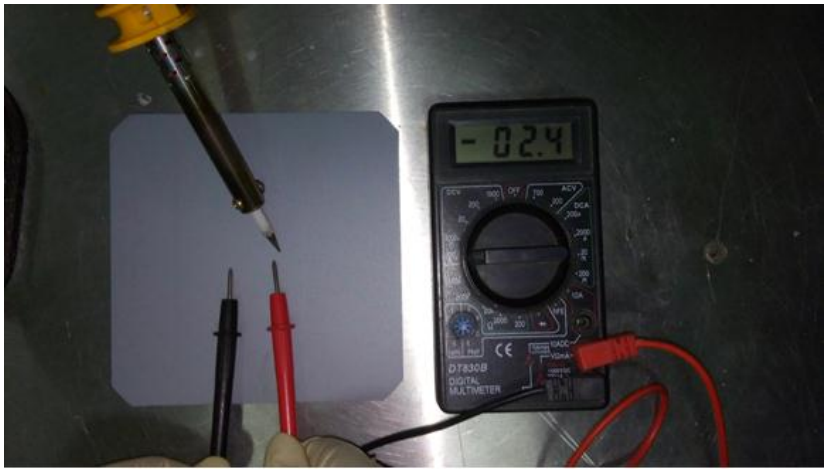

Figure 11.5 "Hot-Probe" Experiment

11.2.5 Four Point Probe Measurement

Four point probe measurement revealed that the sheet resistivity of the as-cut, 200 μm thick, *P*-type pseudo-square mono-crystalline silicon wafer with an area of 150×150 mm^2 substrates lies between 1.12-9.46 Ω.cm. As the doping concentration of the substrate is not uniform, the sheet resistance varies significantly. The sheet resistance of the wafer doped in this research has also been measured. For the doped wafer the diffusion and drive time are 5 min-10 min, 10 min-15 min, 15 min-20 min, 20 min-25 min, 20 min-25 min and 25 min-30 min, respectively. The sheet resistance have been tabulated in Table 11.1. The table shows that highest sheet resistance of 65.25 Ω/□ has been achieved for 5 min diffusion and 10 min drive time. Lowest sheet resistance of 13.53 Ω/□ has been achieved for 15 min diffusion and 20 min drive time. However, solar cell sheet resistance lies between 60-100 Ω/□.

TABLE 11.1: Data for Sheet Resistance

Diffusion 5 min and Drive in 10 min		Diffusion 10 min and Drive in 15 min		Diffusion 15min and Drive in 20 min	Diffusion 20 min and Drive in 25 min		Diffusion 30 min and Drive in 35 min	
Sample1	Sample2	Sample1	Sample2	Sample1	Sample1	Sample2	Sample1	Sample2
Sheet Resistance (Ω/□)	Sheet Resistance (Ω/□)	Sheet Resistance (Ω/□)	Sheet Resistance (Ω/□)	Sheet Resistance (Ω/□)	Sheet Resistance (Ω/□)	Sheet Resistance (Ω/□)	Sheet Resistance (Ω/□)	Sheet Resistance (Ω/□)
50.6	80.2	41.3	48.1	13.6	28.7	37.3	49	61.7
50.4	80	41.1	48.1	13.6	28.1	37.1	49.2	61.8
50.4	79.9	41	48.1	13.4	28.6	36.7	48.9	61.7
Avg. 65.25 Ω/□		Avg. 44.62 Ω/□			Avg. 13.53 Ω/□		Avg. 55.38 Ω/□	

TABLE 11.2: Data for Different Parameter Values of *N*-type Doped Wafer

Diffusion Time and Drive Time	Sheet Resistance (Ω/□)	Thickness (cm)	Ω -cm Sheet Resistivity (Rs)	q Electron Charge (coulombs)	Hole Mobility μ_p ($cm^2/v{\cdot}s$)	Electron Mobility μ_n ($cm^2/v{\cdot}s$)	N Electron Concentration (cm^{-3})	ni Intrinsic Carrier Concentration (cm^{-3})	p0=(ni)2/n Hole Concentration (cm^{-3})
5min, 10 min	65.25	0.0001	0.006525	1.6×10^{-19}	450	1200	7.98×10^{17}	1.5×10^{10}	281.88
10min, 15 min	44.62		0.004462				1.17×10^{18}		192.7584
15min, 20 min	13.53		0.001353				3.85×10^{18}		58.4496
20min, 25 min	32.75		0.003275				1.59×10^{18}		141.48
30min, 35 min	55.38		0.005538				9.4×10^{17}		239.2416

Moreover, depending on time, sheet resistance, carrier concentration and cost 5 min diffusion and 10 min drive time is considered the optimum diffusion recipe. From the sheet resistance electron concentration, hole concentration and other parameters can be theoretically calculated

by using the following two equations. Table 11.2 shows different parameter values including electron concentration, hole concentration of *N*-type doped wafer. It should be mentioned that the hole mobility value is considered from reference [5].

$\sigma = \frac{1}{\rho}$; [σ = Conductivity; ρ = sheet resistance/resistivity (Ω/□ or Ω - cm)] …… (1)

$\sigma = q\,(\mu_n n + \mu_p p)$; …….(2)

[n = Electron concentration (cm^{-3}); p = Hole concentration (cm^{-3});

μ_p = Hole mobility ($cm^2/v{\cdot}s$); μ_n = electron mobility ($cm^2/\ v{\cdot}s$)

[v·s =square centimeter per volt per sec: $cm^2/v^{-1}.\ s^{-1}$];

q = electron charge in coulombs]

11.2.6 Energy Dispersive X-Ray Spectroscopy (EDS)

Energy Dispersive X-Ray Spectroscopy (EDS or EDX) is a chemical microanalysis technique used in conjunction with scanning electron microscopy (SEM) [6]. EDS uses the X-ray spectrum emitted by a solid sample bombarded with a focused beam of electrons to obtain a localized chemical analysis. All elements from atomic number 4 (Be) to 92 (U) can be detected in principle, though not all instruments are equipped for 'light' elements (Z < 10).

When the sample is bombarded by the SEM's electron beam, electrons are ejected from the atoms comprising the sample's surface. The resulting electron vacancies are filled by electrons from a higher state, and an X-ray is emitted to balance the energy difference between the two electrons' states. As the energies of the X-rays are characteristic of the difference in energy between the two shells and of the atomic structure of the emitting element, EDS allows the elemental composition of the specimen to be measured [7]. The EDS X-ray detector measures the relative abundance of emitted X-rays versus their energy. The detector is typically a lithium-drifted silicon solid-state device. When an incident X-ray strikes the detector, it creates a charge pulse that is proportional to the energy of the X-ray. The charge pulse is converted to a voltage pulse (which remains proportional to the X-ray energy) by a charge-sensitive preamplifier. The signal is then sent to a multichannel analyzer where the pulses are sorted by voltage. The energy, as determined from the voltage measurement, for each incident X-ray is sent to a computer for display and further data evaluation. The spectrum of X-ray energy versus counts is evaluated to determine the elemental composition of the sampled volume.

For EDS analysis AMETEK Octane Prime has been used. Before discussing the measured data some understanding of instrument related knowledge is necessary. In the output graph (shown in Appendix-A) the height of the Characteristic X-ray peaks in an ED spectrum, or the X-ray intensity, is given in X-ray counts or count rate (counts per second or cps). In general it is assumed that the height of the X-ray peak in the spectrum will be proportional to the concentration of the element in the sample. For spectra generated from a TEM this is largely true but for spectra generated from an SEM it is not the case. Factors related to the sample, the system used to generate the X-rays and the detector used to measure the X-ray spectrum, all can influence the height of the X-ray peaks. While the intensities of the peaks in an X-ray energy spectrum are not directly proportional to element concentration, it is true that the concentration of the element in the sample will influence the height of the X-ray peak. Elements

present in major amounts (> 10 wt%) will have major peaks in the spectrum while elements present in minor (1-10 wt%) or trace amounts (<1 wt%) will have small or undetectable peaks in the spectrum. In the instrument the beam current (probe current) or spot size reflects the number of electrons in the primary beam of the electron microscope. It is controlled by the condenser lens or the spot size control knob. The number of electrons in the primary electron beam is directly proportional to the number of X-rays generated from the sample and the number of X-ray counts (intensities) recorded in the X-ray spectrum. Increasing the beam current will increase the number of X-rays generated from the sample but will not change the relative heights (intensities) of the Characteristic X-ray peaks in the spectrum. Furthermore, the accelerating voltage used in the electron microscope controls the energy of the electrons in the primary beam. In the SEM, accelerating voltages are typically 5-30 keV but in TEMs much higher accelerating voltages, 100-400 keV or more, are used.

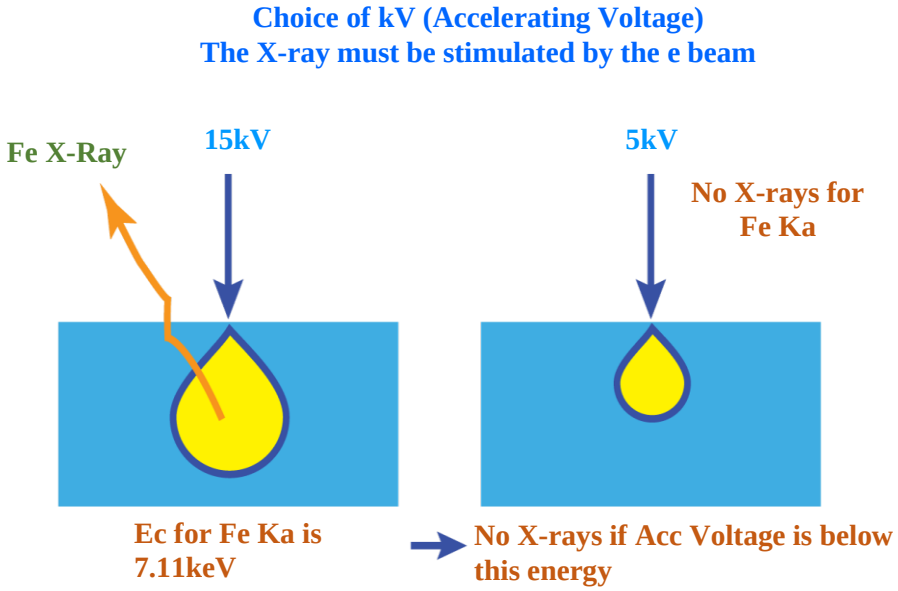

Figure 11.6 X-ray Generation (If the energy of the electrons in the primary beam is less than the critical ionization energy, then no X-rays will be generated. If the accelerating voltage is 15 kV, both K and L family X-rays will be generated from Fe. If the accelerating voltage is 5 kV, no K family X-rays will be produced)

In order to generate Characteristic X-rays, the electrons in the primary beam must have enough energy to overcome the ionization energy, also called the critical ionization energy, of the inner-shell electrons in the atoms of the sample. With the high accelerating voltages used in TEMs this is not a problem, but in SEMs care must be taken to use a sufficiently high accelerating voltage to stimulate X-rays from all elements in the sample (Figure 11.6).

An important term in EDS instrument is overvoltage ratio. The overvoltage ratio is the ratio of the energy of the electrons in the primary beam, E_o, to the critical ionization energy, E_c, needed to ionize an inner shell of an atom in the sample. For example, if the accelerating voltage is 15 kV, the energy of the electrons in the primary beam is 15 keV. The critical excitation energy of the Fe Kα X-ray is 7.11 keV, and therefore the overvoltage ratio, $U = E_o/E_c$, is 2.11. For efficient generation of X-rays, the overvoltage ratio should be at least 2 (the optimum value is ~2.7, Figure 11.7).

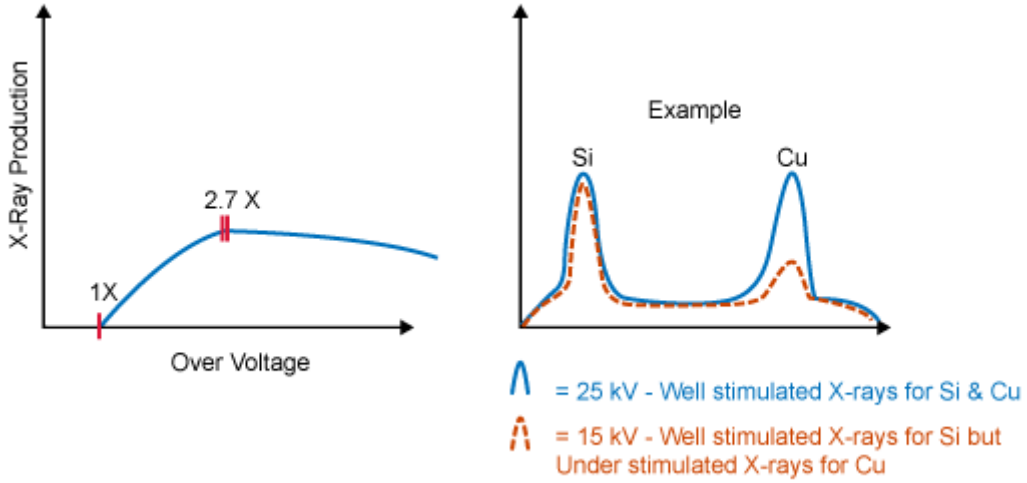

Figure 11.7 Overvoltage Ratio (An overvoltage ratio of at least 2 is needed for efficient generation of X-rays. If low accelerating voltages are used, higher energy X-rays will not be efficiently generated)

Not all of the X-rays that are generated in the sample by the primary electron beam are emitted from the sample. While the absorption of X-rays depends on the other elements present in the sample, it is also true that low-energy X-rays are more likely to be absorbed than those with higher energies, and elements with higher atomic numbers tend to be strong absorbers of lower energy X-rays. The length of the path that the X-ray travels through the sample will also influence absorption. The longer the path length, the more likely it is that the X-ray will be absorbed. Again, low-energy X-rays are more likely to be affected by longer path lengths than higher energy X-rays.

EDS data shows that (Table 11.3) *P*-type wafer has only Boron (B) and Silicon (Si). It thus proves that the material is (Si) and (B) indicates that it is doped and it is *P*-type silicon wafer. It is to be noted that K in the Table 11.3 indicates K type characteristics X-ray.

TABLE 11.3: EDS Data for *P*-type Wafer

Element	Weight %	Atomic %
B K	0.6	1.5
Si K	99.4	98.5

Furthermore, EDS data shows that (Table 11.4) *N*-type doped wafer has Boron (B), Oxygen (O), Phosphorus (P) and Silicon (Si). It thus proves that the material is silicon and phosphorus boron indicates that it is *N*-type layer is formed. Low concentration of boron indicates that there is *P*-type in very depth of the wafer. Oxygen indicates that there is surface passivated layer upon *N*-type layer. The concentration of oxygen is higher for 5kV accelerating voltage and decreasing as accelerating voltage decreases (20 kV). It tells us that increasing accelerating voltage the electrons of electron gun goes deeper and gives more depth information of the material. The surface passivated layer decreases as depth increases. That is why oxygen concentration also decreases.

TABLE 11.4: EDS Data for *N*-type Wafer (5 min Diffusion and 10 min Drive-in)

	5kV (Accelerating voltage)		20 kV (Accelerating voltage)	
Element	Weight %	Atomic %	Weight %	Atomic %
B K	0.4	0.9	0.0	0.0
O K	36.1	49.8	15.9	25.0
Si K	56.0	44.0	82.4	73.7
P K	7.4	5.3	1.7	1.3

11.2.7 Series and Shunt resistance

Series and shunt resistance of the fabricated solar cell has been measured. It is seen that under low light conditions the shunt resistance has been found 234 ohm for a 12.5×12.5 cm^2 wafer, whereas good solar cell has more than 1000 ohm of shunt resistance [9]. (More details are given in Chapter 5 Section 5.2.4).

The series resistance, Rs of the fabricated solar cell is found 6.197 $\Omega.cm^2$. Which is much higher as high efficient solar cell series resistance value varies from 0.3 $\Omega.cm^2$ to 1 $\Omega.cm^2$ [10]. (More details are given in Chapter 5 Section 5.2.5).

11.2.8 LIV Measurement

The light intensity current voltage (LIV) measurement (described in Chapter 3, Section 3.15 in details) has been done to two previously fabricated solar cells. The solar cells are edge isolated with edge isolation paste (More details are given in Chapter 4 Section 4.5). The solar cell numbered 'Sample 1' before edge etching with chemical solutions, result in the following parameters with the LIV test. Maximum power (P_{max}) of 3.80487 mW, Voltage at maximum power (V_{max}) is 0.295434 V, Current at maximum power (I_{max}) is 12.8789 mA, Open circuit voltage (V_{oc}) is 0.606448 V and Short circuit current is (I_{sc}) is 27.201 mA. With these values the *FF* and efficiency of the solar cell are calculated and they are-

$FF = V_m I_m / V_{oc} I_{sc}$ = (0.295434V × 12.8789mA) / (0.606448V) × (27.200mA)

FF = 0.230745

Efficiency (η): $\eta = P_{out}/P_{in}$

= $[(V_{oc} \times I_{sc} \times FF)/P_{in}]$

= [{0.606448V×27.201mA×0.23}/100mw]

= 3.8% [11]

Again, the solar cell numbered 'Sample 2' before edge etching edge etching with chemical solutions, result in the following parameters with the LIV test. Maximum power (P_{max}) is 4.68356 mW, Voltage at maximum power (V_{max}) is 0.320927 V, Current at maximum power (I_{max}) is 14.5939 mA, Open circuit voltage (V_{oc}) is 0.606448 V and Short circuit

current is (I_{sc}) is 29.4258 mA. With these values the *FF* and efficiency of the solar cell are calculated and they are-

$FF = V_m I_m / V_{oc} I_{sc}$ = (0.320927V × 14.5939mA) / (0.606448V) × (29.4258mA)

=0.26241

Efficiency (η): $\eta = P_{out}/P_{in}$

= [($V_{oc} \times I_{sc} \times FF)/P_{in}$]

= [{0.606448V×29.4258mA×0.26}/100mw] ×100%

= 4.6% [11]

So the efficiency of the two solar cells before chemical edge isolation are 3.8% and 4.6%, respectively. Now, the chemical edge isolation process has been applied to the two solar cells. For that HNA solution has been used for 2 min. The ratio of HNA solution is 33ml of Acetic acid: 21ml of nitric acid: 12ml of hydrofluoric acid respectively. Then again efficiency has been measured by LIV test. LIV test of the 'Sample 1' gives the following results. Maximum power (P_{max}) is 5.31341 mW, Voltage at maximum power (V_{max}) is 0.341321 V, Current at maximum power (I_{max}) is 15.5672 mA, Open circuit voltage (V_{oc}) is 0.586054 V, and Short circuit current is (I_{sc}) is 30.8163 mA. With these values the *FF* and efficiency of the solar cell are calculated and they are-

$FF = V_m I_m / V_{oc} I_{sc}$ = (0.341321V × 15.5672mA) / (0.58654V) × (30.8163mA)

=0.29405

Efficiency (η): $\eta = P_{out}/P_{in}$

= [($V_{oc} \times I_{sc} \times FF)/P_{in}$]

= [{0.586054V×30.8163mA×0.29}/100mw] ×100%

= 5.31% [11]

LIV test of the 'Sample 2' gives the following results. Maximum power (P_{max}) is 5.31246 mW, Voltage at maximum power (V_{max}) is 0.31073 V, Current at maximum power (I_{max}) is 17.0967 mA, Open circuit voltage (V_{oc}) is 0.591152 V, and Short circuit current is (I_{sc}) is 31.1871 mA. With these values the *FF* and efficiency of the solar cell are calculated and they are-

$FF = V_m I_m / V_{oc} I_{sc}$ = (0.31073V × 17.0967 mA) / (0.591152V) × (31.1871 mA)

=0.28825

Efficiency (η): $\eta = P_{out}/P_{in}$

= [($V_{oc} \times I_{sc} \times FF)/P_{in}$]

= [{0.591152 V ×31.1871 mA×0.29}/100mw] ×100%

= 5.34% [11]

So the efficiency of the two solar cells after chemical edge isolation are 5.31% and 5.34% respectively. So definitely proper edge isolation is not done before. However, chemical edge isolation is difficult and dangerous. Most of the time the fumes of chemicals causes change in the *N*-type layer. So it is suggested to used Microwave Plasma System [12]. Where edge isolation is done by stacking the wafers on top of each other and producing plasma with microwave frequency 2.45 GHz and having an etching environment consists of combination of fluorinated gas (CF_4) and oxidant gas (O_2).

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Chapter 12

CONCLUSION

12.1 Fabrication of Monocrystalline Silicon Solar Cell in Bangladesh

The fabrication process of monocrystalline silicon solar cell in Bangladesh started with a 200 μm thick, *P*-type pseudo-square monocrystalline silicon wafer with an area of 150×150 mm^2 [1]. Due to availability and because the efficiency of solar cell is best for monocrystalline silicon wafer, this type of wafer is chosen for fabrication. Now to remove the saw damage and to clean the wafers, the wafers are submerged in 10% NaOH solution at 70-80°C for 10 min. Then the wafers are dried with air-guns. Next the texturization process is carried out using KOH-IPA solution with 0.76 wt% KOH-4 wt% IPA concentration. The texturization process temperature is conducted with temperature between 70°C to 80°C for 20 min because 20 min showed the best result [2-5]. Once the texturization process is done the wafers are dried again with air-guns. Then the textured wafers are inserted in the atmospheric pressure chemical vapor deposition (APCVD) chamber. N_2 gas, O_2 gas and liquid Phosphorous Oxicloride ($POCl_3$) are used in the APCVD chamber to create *N*-type layer upon *P*-type layer [6-7]. Furthermore, the flow meters of the APCVD chamber is adjusted to 14.7 psi (1 atm) to operate. The deposition and drive-time process are 5 min and 10 min respectively (More details are discussed in Chapter 10 Section 10.3). It is seen that after diffusion process is done *N*-type layer is formed upon *P*-type wafer and *P*-*N* junction is formed. Then the diffused wafer is placed in the vacuum table of the screen printing machine. Although the screen printing machine does not work, the vacuum table of the screen printing machine works well. Hence, it is used to hold the diffused wafer in the vacuum table. After that the screen printing process is done manually. Suzhou Kaiyuan Minsheng Sci & Tech Corp. Ltd. sliver and aluminum paste (MSR67:03N160503 and MAR6301E:01E160728-1) has been used in the screen printing process. After that busbar and Grid finger and back contact printing is manually done each time the screen printed wafer is dried in the dryer oven at 150°c for 10 min. Then the wafer is inserted in the conveyor belt furnace. The temperature zones of conveyer belt furnace are 500°C, 600°C and 800 °C. The inch per minute (ipm) of conveyer belt furnace is set at 22. It takes almost four and a half minute for the wafer to come out of the furnace. The conveyer belt furnace ipm vs. time chart table is given in Table 12.1. After completion of co-firing in conveyer belt furnace metallization process is completed and the wafers are required to cool down. The locally fabricated solar cells are shown in Figure 12.1. Unfortunately the solar cells efficiency could not be measured. Because there might be problems in the LIV test equipment as there is no calibrated solar cell or the solar cell *P*-*N* junction is short circuited. The *P*-*N* junction is/may be short circuited because of the conveyer belt furnace. As there is no option to apply oxygen and nitrogen gas in the conveyer belt furnace which is required during metallization process. Also the wafer staying the conveyer belt furnace is too long. Not more than 30 sec the wafers should stay in the furnace. But the ipm of the furnace does not work that fast. Although due to the limitation of fabrication equipments proper solar cell is not fabricated however simulation of efficient solar cell has been done in Bangladesh.

TABLE 12.1 Conveyer Belt Furnace ipm vs. Time Chart

Inch Per Minute (ipm)	Time
20	4 min 27 sec.
35	2 min 30 sec.
45	1 min 58 sec.
60	1 min 30 sec.

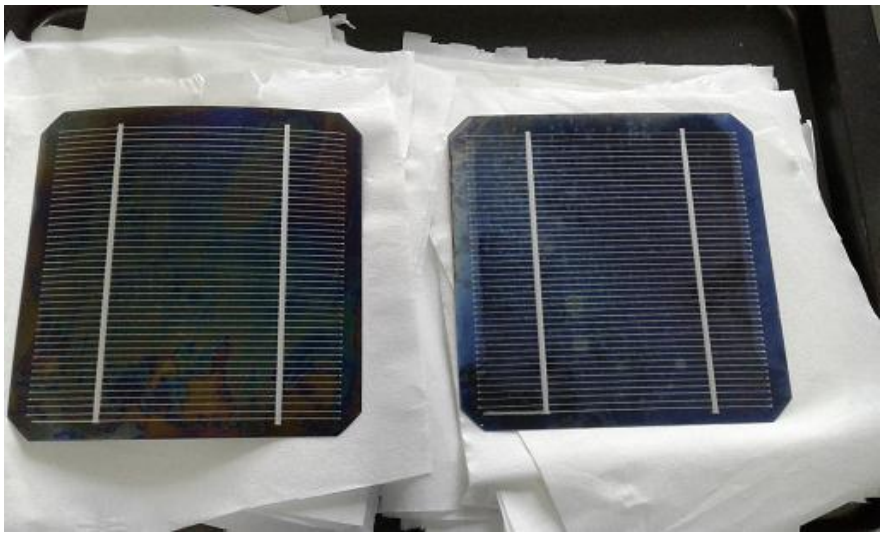

Figure 12.1 Locally Fabricated Solar Cell

12.2 Proposals to Improve Efficiency of Monocrystalline Silicon Solar Cell Fabricated in Bangladesh

To fabricate proper solar cell in Bangladesh the following requirements are absolutely necessary [8].

12.2.1 Clean Room

Modern solar cell manufacturing is performed in a sophisticated room known as a clean room. In general International Standards Organization (ISO) ISO 5 – ISO 6 class room is needed for fabrication of solar cell. Thus, it is proposed to have a clean room of that standard for the solar cell fabrication laboratory in Bangladesh.

12.2.2 Edge Isolation

Use of edge isolation paste is one of the main reason for achieving low efficiency solar cell in Bangladesh and using wet chemicals for edge isolation is very difficult, dangerous and not a permanent solution. So for better performance in the edge isolation process it is proposed to use Microwave Plasma System [9]. Where edge isolation is done by stacking the wafers on top of each other and using, plasma with microwave frequency 2.45 GHz and having an etching environment consists of combination of fluorinated gas (CF_4) and oxidant gas (O_2).

12.2.3 Anti-Reflection Coating

Antireflection coating (ARC) is a layer on the surface of solar cell (On *N*-type layer) to reduce the reflection of sunlight. But no anti-reflection coating is used in fabricating solar cell in Atomic Energy Research Establishment (AERE) laboratory. Silicon nitride (SiNx) layer is the most widely used materials as ARC. Furthermore, simulation (Chapter 7, Section 7.3) shows silicon nitride ARC has the best result. So purchasing silicon nitride ARC related equipment is mandatory step to improve the efficiency of solar cell.

12.2.4 Wafer Selection

The first step of making silicon solar cell is choosing the *P*-type silicon wafer. From the study and simulation it can be found that a 300 μm thick wafer with uniform doping will increase the efficiency. Float Zone (FZ) wafer will be a good choice instead of Czochralski (CZ) wafer.

12.2.5 Diffusion Furnace

Improper diffusion causes un- uniform doping and poor efficiency of solar cell. This can be avoided if the chamber has a flow-meter to control gas rate. Also, automated system provide better gas control option. Hence, the use a better diffusion chamber will give better performance.

12.2.6 Screen Printing

Proper screen printing causes good aspect ratio in busbars and grid fingers and this can improve the efficiency of solar cell. So automated screen printing machine is needed for solar cell fabrication.

12.2.7 Silver and Aluminum Paste

If better quality silver and aluminum paste is used for the busbars and grid-fingers of solar cell efficiency can be increased. In the silver and aluminum paste the composition of silver and aluminum must be more than 80%.

12.2.8 Conveyer Belt Furnace

Proper metallization is one crucial step in solar cell fabrication process. Thus conveyer belt furnace should have the option to provide oxygen (O_2) and nitrogen (N_2) gas during metallization process. Furthermore flow meter is needed to control the gas flow rate. Conveyer belt moving speed that is inch per minute (ipm) must be variable and should be such that the whole process can be completed within 30 sec.

12.2.9 Characterization Equipment's

Characterization equipment identifies various solar cell parameters, which helps the scientists and researchers to understand the performance of solar cell and take necessary changes to improve the solar cell parameters thus increasing the efficiency of solar cells. A solar cell fabrication laboratory must have a characterization equipment section. The section will contain all the solar cell characterization equipment. The distance between fabrication and characterization laboratory should be minimum. The following equipment's are necessary for the monocrystalline solar cell characterization laboratory. The light intensity (L), current (I) and voltage (V) (LIV) tester (for efficiency measurement), Scanning Electron Microscope (SEM), High Resolution Optical Microscope, Ultraviolet-Visible-Near Infrared (UV-VIS-NIR) Spectrophotometer, Four Point Probing *I-V* Measurement System, Energy Dispersive

Spectroscopy (EDS) system, Hall-Effect Measurement System, Surface Profilometer, Deionized Water Plant, Spin Coter, Atomic Force Microscopy (AFM), Infrared camera electroluminescent crack detection equipment and Surface Photovoltage Measurement System. All the systems needs individual computers or data logging facilities.

12.2.10 Wet Chemical Bench

The wet chemical bench should be automatized. Because automation gives good and uniform rinsing of wafers with chemicals. Also, mixing of chemicals and proper heating is done with automation. Exhaust system must be good so that the chemical fumes does not enter anywhere but the exhaust chamber.

12.2.11 Automated Solar Cells Tabbing Machine

The line resistance of a tab is typically 20 times better than that of a screen printed busbar [8]. Thus tabbing is necessary and that is why an automated solar cells tabbing machine is needed. Also with tabbed solar cell, the solar cell can be directly used under the sun.

12.2.12 Parameter Values

Series resistance, shunt resistance, minority carrier diffusion length and aspect ratio of busbars and grid-fingers of the locally fabricated solar cell must be improved.

12.2.13 Front and Back Contact Metallization

The solar which has been fabricated in the Atomic Energy Research Establishment (AERE) laboratory has two busbars, but as 12.5×12.5 cm^2 solar cell is quite big [10] using of 3 busbars instead of 2 busbars in front contact metallization process will increase the efficiency of solar cell. Because applying 3 busbar in front contact layout design will improve current collection because of lower electric resistance. Also, for back contact metallization along with aluminum paste discontinues silver busbars should be used. The discontinues silver busbars should be of 2 strips with 3 gaps, or 3 strips with 3 gaps on each busbar on the back side.

12.2.14 Different Design Approach

To improve the efficiency of solar cell it is suggested not to follow the standard solar cell design but to follow any of the following design. PERL (Passivated Emitter, Rear Locally-diffused) solar cell, buried contact solar cell, bi-facial cell, Passivated Emitter Rear Contact (PERC) solar cell etc.

12.2.15 Surface Passivation

It is well known that, high surface recombination rate reduces short circuit current and thus the efficiency of solar cells. Surface passivated layer should have a thickness about 100 nm to get better efficiency.

12.3 Achievements

There are a few crucial achievements of this PhD research work. These are listed below.

- Problem analysis of monocrystalline silicon solar cell fabricated in the one and only monocrystalline silicon solar cell laboratory at Atomic Energy Research Establishment (AERE), Savar, Bangladesh has been done [11]. The explored problems will help to

take appropriate measures to improve the efficiency of solar cell. Problem analysis of the locally developed monocrystalline silicon solar cell fabricated in Bangladesh has been detailed discussed in Chapter 5.

- 20.67% efficient solar cell has been simulated using PC1D simulation software [12] (Chapter 6 and 7 for details).
- Impact of six different anti-reflection coating (ARC) layer has been investigated using PC1D simulation software. Also efficient solar cell modelling with optimum efficiency has been achieved by using SiO_2 surface passivation and Si_3N_4 ARC layer [12-13] (Chapter 7 for details).
- Different texturization experiment on processes have been practically applied and studied. Optimized texturization recipe is obtained. Within 250-800 nm wavelength range, 0.1-0.026% absolute reflectance has been achieved when textured with 0.76 wt% KOH-4 wt% IPA solution for 20 minutes. (Chapter 9 for details).
- Band gap of *P*-type monocrystalline silicon wafer has been measured using spectral response measurement system and with a unique approach [14-15]. (See chapter 8 for details.)
- Optimum diffusion time (5 min) and drive time (10 min) has been determined practically [7]. (Chapter 10 for details).
- Various parameters of fabricated solar cell have been obtained after characterization. (Chapter 11 for details).
- During this PhD research work total 17 publications have been done. Out of 17 publications, 8 are journal publication, 8 of them are conference publications and one is a poster presentation. Among all the journals, three journals have been published in the **Springer**. (All the publications are given in the "Publication List", page VII).

12.4 Conclusion

Use of photovoltaic energy is increasing all over the world including Bangladesh. Bangladesh has become world model by establishing 4.5 million solar home systems so far (by 2018). Some of the companies are assembling PV module locally, but unfortunately all the solar cells of the PV modules are imported from abroad. For this reason, the main goal for this research is to fabricate efficient solar cell locally. Fabrication method of monocrystalline silicon solar cell has been thoroughly studied and described in this research work. Fabrication steps include cleaning, surface texturing, edge isolation, diffusion, screen printing and co-firing process. The efficiency of the solar cell fabricated in Bangladesh is very low, that is 6.89% (up to date). So it is very important to identify the problems of fabrication to enhance the efficiency. Thus the problems of the fabricated monocrystalline silicon solar cell have been investigated and determined. The problems are:

- Not having ISO standard clean room
- Improper edge isolation
- Wafer bowing
- Low shunt resistance
- High series resistance (6.197 $\Omega.cm^2$)

- Low minority carrier life time (88 µm)
- Not applying ARC layer
- Micro cracks in busbars etc.

The uniformity of the busbars and grid-fingers of the locally manufactured solar cells have been studied using Dektak 150 Surface Profiling System. The measurement shows more unevenness and less aspect ratio in the locally fabricated solar cell. Moreover, oxygen and nitrogen gas has not been used in metallization process during fabrication, which is one of the reasons for wafer bowing and micro cracks in busbars. So it is seen that there are a lot of problems in the locally fabricated solar cell. In this research work, in addition to investigate the limitations of the fabrication process, some remedies to the problem have been found practically and by simulation.

In all the cases of solar cell fabrication, the experimental procedure is difficult for understanding, sometimes phenomena are not observable or measurements are impractical. Furthermore, little change in the solar cell fabrication process is too expensive. Because, change in any aspect of fabrication process is a difficult task, simulation of monocrystalline silicon solar cell has been done using PC1D software. At first simulation of monocrystalline silicon solar cell using PC1D shows that, for a *P*-type monocrystalline silicon wafer, with area of 10×10 cm^2 and a thickness of 300 micrometer, solar cell efficiency is 12.10%. After optimization of solar cell parameters, that is considering *P*-type doping concentration 1×10^{17} cm^{-3}, *N*-type doping concentration 1×10^{18} cm^{-3}, diffusion length 200.3 nm, both side textured wafer with pyramid height 3 micrometer and angle of 54.74 degrees and with anti-reflection coating thickness of 74 nm and refractive index 2.019, 20.35% efficiency has been achieved. Simulation also shows that, textured surface reduces reflection and increase efficiency of solar cell at least 1-2%. Furthermore, impact of six different anti-reflection coating (ARC) layer has also been investigated using PC1D simulation software. Simulation shows that the range of 500 nm – 700 nm would be suitable for designing an ARC. Designing a single layer silicon nitride (Si_3N_4) ARC for 600 nm wavelength and with a thickness of 74.257 nm, a silicon solar cell with 20.35% efficiency has been simulated. Very closely followed by a 20.34% efficient silicon solar cell with 74.87 nm thick Zinc oxide (ZnO) ARC layer. Significant increase in efficiency has been observed by applying ARC compared to the cell without any kind of ARC. After efficient solar cell modelling, optimum efficiency of 20.67% is being achieved by using SiO_2 surface passivation and Si_3N_4 ARC layer. Increase in EQE and decrease in reflectance also confirms that surface passivated layer upon ARC increases the efficiency of solar cell.

As band gap measuring equipment are very costly and not available in Bangladesh. For this purpose, in this research work it has been done in a different way. Although, the primary purpose of spectral response measurement system is to measure the spectral response of a material, this system has been used to measure the band gap of *P*-type monocrystalline silicon wafer. The measurement shows that, the band gap of polished *P*-type monocrystalline silicon wafer is 1.127907 eV. Whereas, theoretically calculated value is 1.127362 eV. As error is 0.04834%, it can be considered as negligible.

Texturing process has been applied on a 200 µm thick, as-cut monocrystalline silicon wafer using 0.763 wt% KOH - 4 wt% IPA, 1.869 wt% KOH - 4.673 wt% IPA, 11.8 wt% Na_2CO_3 - 1.5 wt% $NaHCO_3$, 1 wt% Na_2CO_3 - 0.2 wt% $NaHCO_3$ and 1 wt% TMAH - 4 wt% IPA solution with different time durations. Texturization process on the monocrystalline silicon substrate

reduces reflection and enhances light absorption of the substrate. Thus, texturization is one of the key steps to increase the efficiency of solar cell. Since there are lot of texturization recipes, research has been done to find out the optimum recipe for texturization based on timing, concentration and temperature. Apart from texturization process, saw damage removal process has also been investigated. Saw damage removal process is completed prior to texturization process with different wet chemical solutions. Here for saw damage removal process, 10% NaOH, 20 wt% KOH - 13.33 wt% IPA and HNA (Hydrofluoric acid, Nitric acid and Acetic acid) solution with different time durations has been used**.** Saw damage removal process using 10 min NaOH solution shows the lowest reflectance. Moreover, the price of NaOH is comparatively lower. Hence, for all the texturization process 10% NaOH solution has been used in saw damage removal process. Furthermore, it is seen that after saw damage removal, almost square shape patterns are formed upon the surface of silicon wafer. Results of different texturization process indicates that very low reflectance can be achieved by using 0.763 wt% KOH - 4 wt% IPA solution**.** This low reflectance is due to the formation of proper pyramidal microstructures on the surface of silicon wafer. These pyramidal microstructures have been observed via FE-SEM. Measurement shows that the height of the pyramid on the silicon surface varies from 1.5 µm to 3.18 µm and inclined planes of the pyramids are acute angle. Contact angle is slightly above 90°. Which indicates that the textured wafers surface falls in the near hydrophobic to hydrophobic range. It is observed that an alternative to 0.763 wt% KOH - 4 wt% IPA solution is 1 wt% Na_2CO_3 - 0.2 wt% $NaHCO_3$ solution with etching time 50 min. Reflectance measured for this solution is not as low as 0.763 wt% KOH - 4 wt% IPA solution but still the textured substrate reflectance is very low and the chemicals used in this process are less harmful and much safer to handle. As wet chemical processing can be scaled up with low manufacturing cost and at the same time the texturization recipes (0.763 wt% KOH - 4 wt% IPA or 1 wt% Na_2CO_3 - 0.2 wt% $NaHCO_3$) yield very low reflectance, any of these texturization processes can be used in monocrystalline silicon solar cell fabrication to reduce reflectivity and enhances light absorption.

The *N*-type layer formed upon *P*-type layer has a vast impact on silicon solar cell performance. Thus formation of *N*-Type layer (Emitter) over an as-cut monocrystalline *P*-type silicon wafer (Base) has been formed by diffusion process. Here, the diffusion process has been carried out at 875 °C in an Atmospheric Pressure Chemical Vapor Deposition (APCVD) chamber by $POCl_3$ (Phosphorus Oxychloride), N_2 and O_2 gas. Where, the deposition time and drive time variations are 5, 10, 15, 20, 30 min and 10, 15, 20, 25 and 35 min respectively. After diffusion hot point probe experiment has been executed and it ensures that *N*-Type layer has been formed. Experimentally obtained values of the emitter sheet resistance are as follows 65.25 Ω/□, 44.62 Ω/□, 13.53 Ω/□, 32.75 Ω/□ and 55.38 Ω/□. From the sheet resistance values electron concentration has been theoretically calculated. For 15 min of deposition the electron concentration is the highest, which is 3.85×10^{18} cm^{-3}. Whereas, the lowest concentration value of electron is 7.98×10^{17} cm^{-3} and it is found for 5 min of deposition. As in fabricated solar cell, the emitter sheet resistance lies in between 50-100 Ω/□ and considering low manufacturing cost, 5 min diffusion and 10 min drive time provides the suitable recipe to create a *N*-type layer upon *P*-type silicon substrate.

Apart from fabrication, characterizations of different silicon wafer and solar cell has been done. The characterization are as follows:

- Surface morphology determination using optical microscope and SEM

- Surface roughness and height determination using surface profilometer
- Band gap measurement using spectral response measurement machine
- Fill factor and efficiency measurement using LIV tester
- Series and shunt resistance measurement
- Sheet resistance determination using four point probe system
- *P*-type and *N*-type determination using hot probe method
- Thickness measurement of different wafers using dial indicator
- Reflectance measurement different wafers using UV-VIS-NiR spectroscopy
- Busbars and grid fingers height, width and aspect ratio measurement
- EDS of different doped wafer.

Solar cell has been fabricated in the Atomic Energy Research Establishment (AERE) laboratory, Bangladesh during this research work as shown in Figure 12.2. Unfortunately the solar cells efficiency could not be measured. Because the LIV tester could not work for not having specific calibrated solar cell. Although, efficient solar cell has not yet been fabricated due to lack of fabrication equipment, efficiency improvement of solar cell has been done using simulation software.

Figure 12.2 Fabricated Monocrystalline Silicon Solar Cell

Furthermore, by using a new texturing recipe low reflectance (better than previous recipe) has been practically achieved. Low reflectance will surely will increase some efficiency of solar cell. Also, several ARC simulation shows promising result to increase the efficiency of solar cell. Furthermore necessary steps to improve the efficiency of solar cell in Bangladesh have been given [8,11,16]. Thus, it can be said that the goal of this PhD thesis has been achieved.

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Appendix

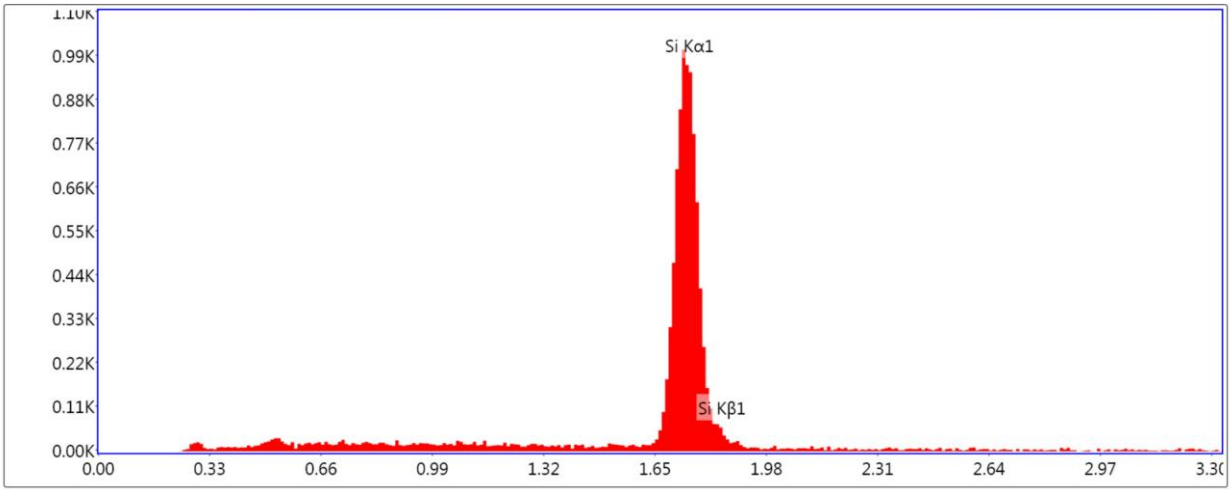
(Data for Raw Wafer, 5kV EDS Measurement)

EDAX TEAM

Full Area 1

kV: 5	Mag: 10000	Takeoff: 34.7	Live Time(s): 50	Amp Time(µs): 7.68	Resolution:(eV)

Full Area 1



Lsec: 50.0 0 Cnts 0.000 keV Det: Octane Prime Det

eZAF Smart Quant Results

Element	Weight %	Atomic %	Net Int.	Error %	Kratio	Z	R	A	F
B K	0.6	1.5	0.0	100.0	0.0009	1.1862	0.9211	0.1316	1.0000
SiK	99.4	98.5	156.9	6.5	0.9949	0.9989	1.0003	1.0000	1.0017

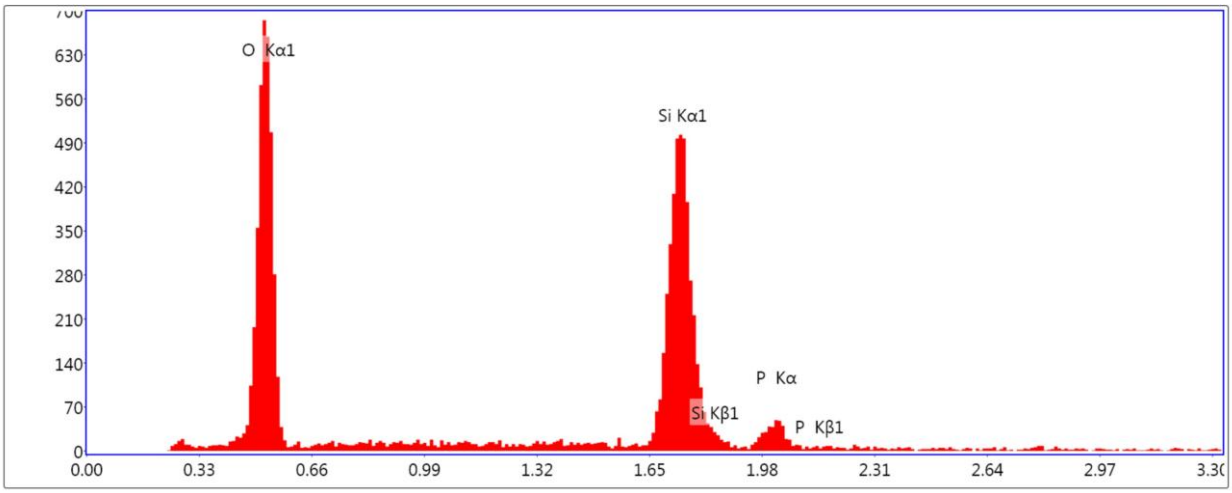
(Data for 5 min Diffusion and 10 min Drive Time *N*-type Doped Wafer, 5kV EDS Measurement)

EDAX TEAM

Full Area 1

kV: 5	Mag: 10000	Takeoff: 34.8	Live Time(s): 50	Amp Time(µs): 7.68	Resolution:(eV)

Full Area 1



Lsec: 50.0 0 Cnts 0.000 keV Det: Octane Prime Det

eZAF Smart Quant Results

Element	Weight %	Atomic %	Net Int.	Error %	Kratio	Z	R	A	F
B K	0.4	0.9	0.0	100.0	0.0010	1.1323	0.9398	0.1919	1.0000
O K	36.1	49.8	70.6	7.6	0.3208	1.0953	0.9730	0.8117	1.0000
SiK	56.0	44.0	78.1	7.3	0.5287	0.9496	1.0109	0.9900	1.0039
P K	7.4	5.3	6.2	18.7	0.0638	0.9057	1.0142	0.9431	1.0032

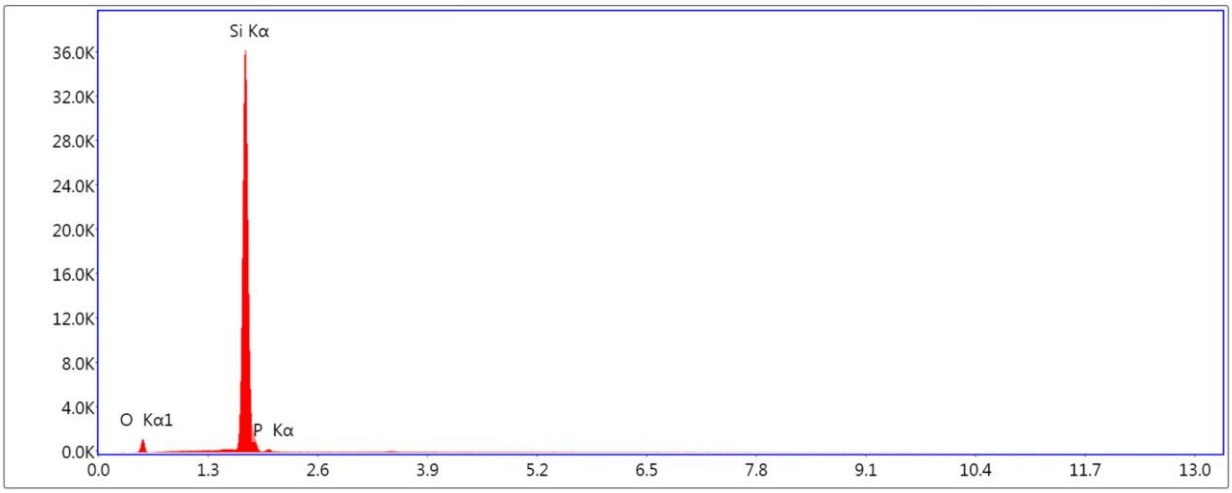
(Data for 5 min Diffusion and 10 min Drive Time *N*-type Doped Wafer, 20kV EDS Measurement)

EDAX TEAM

Full Area 1

kV: 20	Mag: 5000	Takeoff: 32.5	Live Time(s): 50	Amp Time(µs): 7.68	Resolution:(eV)

Full Area 1



Lsec: 50.0 0 Cnts 0.000 keV Det: Octane Prime Det

eZAF Smart Quant Results

Element	Weight %	Atomic %	Net Int.	Error %	Kratio	Z	R	A	F
B K	0.0	0.0	0.0	100.0	0.0000	1.0696	0.9214	0.0567	1.0000
O K	15.9	25.0	122.4	10.2	0.0376	1.0798	0.9572	0.2189	1.0000
SiK	82.4	73.7	5635.9	1.7	0.7663	0.9845	1.0071	0.9421	1.0022
P K	1.7	1.3	38.4	11.4	0.0063	0.9458	1.0138	0.4046	1.0029